MULTI LINE UNIT

DLV 11 J

V 900.610

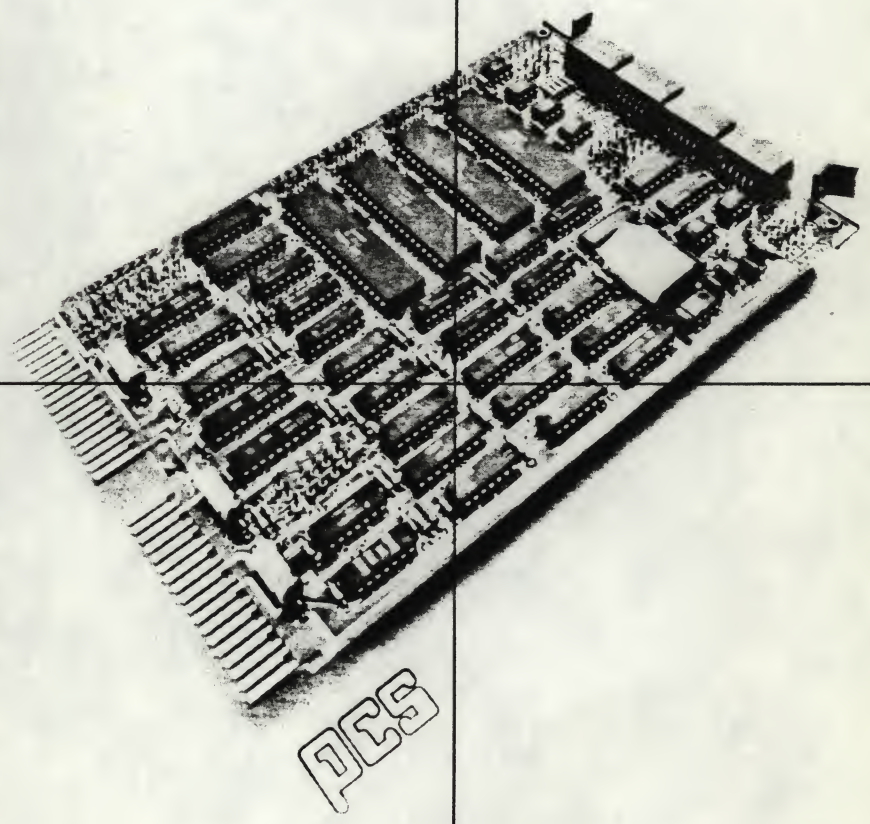
PCS

Periphere
Computer Systeme GmbH

Vier-Kanal asynchrones, serielles-Interface

Die DLV 11-J dient als Interface zwischen 4asynchronen, seriellen Kommunikations-nälen und dem Q-Bus im SII Rechner. e führt Seriell/Parallel- und Parallel/Seriell-Datenkonversionen mit je einem universellen asynchronen Empfänger/Sender (UART) pro Kanal durch. Der UART enthält alle Sender- und Empfängerfunktionen. Der Empfänger führt die Seriell/Parallel-Konversion von 7- oder 8-Bit-Codes durch, die Zeichen erscheinen im Datenpuffer rechtsbündig ohne Start-, Stop- und Paritätsbits. Der Sender führt die Parallel/Seriell-Konversion der Daten, die vom Q-Bus kommen aus und versieht diese mit Start-, Stop- und Paritätsbits. Die PCS 900610 enthält 16 Device-Register, die vom Programm individuell adressiert werden können.

PCS 900.610



Für jeden Kanal (0-3) gibt es die

Empfangs-Kontroll/Status-Register	(RCSR)
Empfangsbuffer	(RBUF)
Sende-Kontroll/Status-Register	(XCSR)
Sendebuffer	(XBUF)

Technische Daten:

- Vier unabhängige serielle Kanäle in einem Bus-Device
- Kompatibilität mit serieller EIA RS-232C und RS-423, AS 422 oder 20 mA Linienstrom (abhängig von Kanalkonfiguration und Kabelauswahl)
- Alle Kanäle können unabhängig voneinander konfiguriert werden: intern quarzgesteuerte Baud-Raten: 150, 300, 600, 1200, 2400, 4800, 9600, 19200 oder 38400 Baud
- extern gesteuerte Baud-Rate

Zeichenformate:

7 oder 8 Datenbits, 1 oder 2 Stopbits, bei Bedarf Parität (ungerade oder gerade)

- Kanal 3 kann der Systemkonsole zugeordnet werden
- Bei Empfang eines „breaks" auf Kanal 3 kann der Prozessor in den Halt-Mode gehen oder einen Bootstrap durchführen.
- Hard- und Software äquivalent zu vier PCS 900615.

Größe	Dual Slot
Stromversorgung	+ 5V / 1A + 12V/0,25A
normierte Busbelastung	1.0 AC, 1.0 DC

Option

Linienstrom-Pegelwandler für 4 Kanäle. Umsetzung von V24 auf 20mA Linienstrom (bis 9600 Baud)

PCS Periphere Computer Systeme GmbH · Pfälzer-Wald-Straße 36 · D–8000 München 90 · Telefon 089/68 10 21 · Telex 5 23 271

MILTI LINE UNIT

DLV 11 J

D 900.610

Beschreibung siehe:

Microcomputer Interfaces Handbook

DLV11-J
Four Asynchronous Serial Interfaces
900.610

Allgemeines

Die DLV11-J dient als Schnittstelle zwischen 4 asynchronen, seriellen I/O-Geräten mit V24-Anschluß und dem LSI11-Bus (Q-Bus).
Werden 20 mA Stromschleifen benötigt, so ist ein zusätzlicher Konverter (DLV11-KA) zu installieren.

Features

- Vier unabhängige serielle Kanäle in einem Bus-Device
- Kompatibilität mit serieller EIA RS-232C und RS-423, AS-422 oder 20 mA Stromschleife (abhängig von Kanalkonfiguration und Kabelauswahl)
- Alle Kanäle können unabhängig voneinander konfiguriert werden:
  für quarzgesteuerte Baud-Raten:
  150, 300, 600, 1200, 2400, 4800, 9600, 19200 oder 38400 Bits pro Sekunde. Bei Anwendung der DLV11-KA Option sind 110 Bit/s verfügbar
  für Zeichenformate:
  7 oder 8 Datenbits, 1 oder 2 Stopbits, bei Bedarf Parität (ungerade oder gerade)
- Kanal 3 kann dem Bildschirminterface gewidmet werden.
- Kanal 3 kann bei Empfang eines 'breaks' entweder in den Halt-Mode gehen oder einen Bootstrap durchführen (auch keine Antwort ist möglich).
- Hard- und Softwareäquivalenz mit vier DLV11en

Spezifikationen

Identifikation	M8043
PCS-Nummer	900.610
Größe	Double Slot
Stromversorgung	+ 5V / 1 A
	+12V / 0,25A
normierte Busbelastung	1,0 AC, 1,0 DC

Funktionsbeschreibung

Die DLV11-J dient als Interface zwischen 4 asynchronen, seriellen Kommunikationskanälen und dem Q-Bus. Sie führt Seriell/Parallel- und Parallel/Seriell-Datenkonversionen mit einem universellen asynchronen Empfänger/Sender (UART) pro Kanal durch. Der UART enthält alle Sender- und Empfängerfunktionen. Der Empfänger führt die Seriell/Parallel-Konversion von 7- oder 8-Bit-Codes durch, die Zeichen erscheinen im Datenpuffer rechtsbündig ohne Start-, Stop- und Paritätsbits. Der Sender führt die Parallel/Seriell-Konversion der Daten, die vom LSI11-Bus kommen, aus und versieht diese mit Start-, Stop- und Paritätsbits.

Register

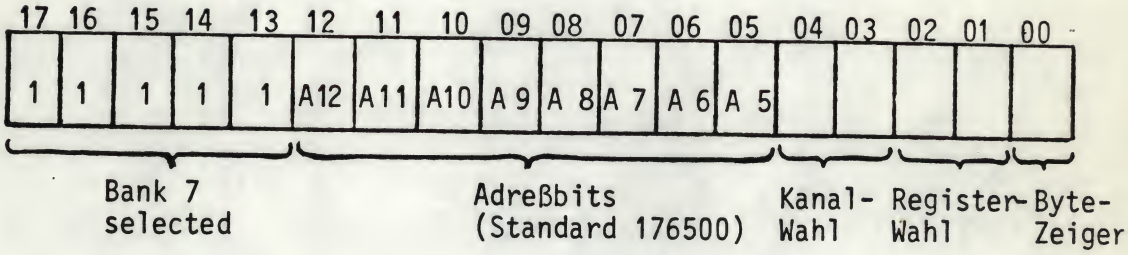
Allgemeines

Das folgende Kapitel enthält die für den Programmierer erforderliche Information über die Bedeutung der einzelnen Register und ihrer Bits.

Die DLV11-J enthält 16 Device-Register, die vom Programm individuell adressiert werden können. Für jeden Kanal (0-3) gibt es die

Empfangs-Kontroll/Status-Register	(RCSR)
Empfangsbuffer	(RBUF)
Sende-Kontroll/Status-Register	(XCSR)
Sendebuffer	(XBUF)

Über die Wire-Wrap-Jumpers läßt sich eine Basisadresse erzeugen. Dies ist das RCSR im Kanal Ø.
Bild 1 zeigt das Format der Device-Adresse sowie das Vektorformat.



Kanal-Wahl:	Adresse	Kanal
	00	0
	01	1
	10	2
	11	3

Register-Wahl:	Adresse	Register
	00	RCSR
	01	RBUF
	10	XCSR
	11	XBUF

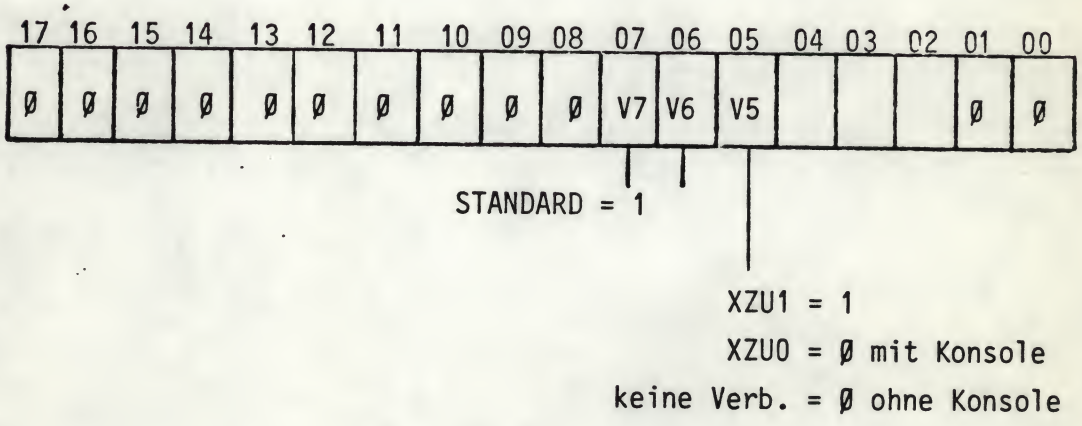


Bild 1

Die verbleibenden Device-Adressen folgen in 16 aufeinanderfolgenden Wortadressen. Es ist jedoch möglich, die letzten vier Adressen (Kanal 3) unabhängig dem Bildschirmterminal zuzuordnen. In diesem Falle wird die Adresse 177560-177566 sein. Soll ein Bildschirm betrieben werden, so muß die Device-Basis-Adresse eine der folgenden sein:

176500, 176540, 177500

Bild 2 zeigt die allgemeine Adreßbelegung, Bild 3 die Standardadressen.

Adresse	Device-Register	zugeordneter Vektor
	Kanal Ø	
Basis-Adresse (BA)	RCSR	Basis-Vektor (BV)
BA+2	RBUF	
BA+4	XCSR	BV+4
BA+6	XBUF	
	Kanal 1	
BA+10	RCSR	BV+10
BA+12	RBUF	
BA+14	XCSR	BV+14
BA+16	XBUF	
	Kanal 2	
BA+20	RCSR	BV+20
BA+22	RBUF	
BA+24	XCSR	BV+22
BA+26	XBUF	
	Kanal 3	
177560	RCSR	60 } Konsole
177562	RBUF	
177564	XCSR	64 }
177566	XBUF	

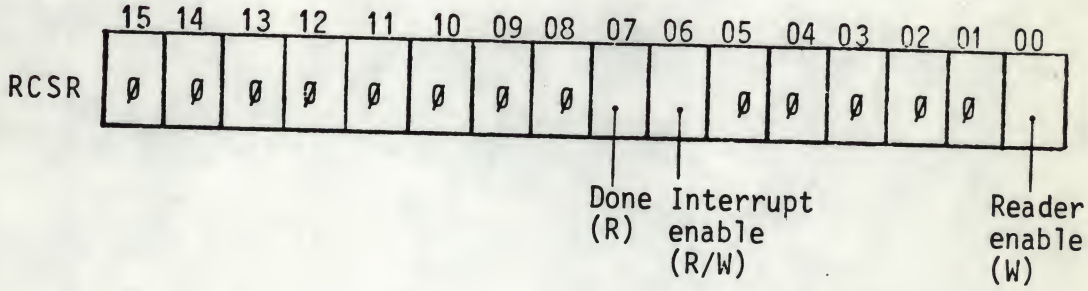
Bild 2

Adresse	Register	Vektor	
176500	RCSR	300	
176502	RBUF		Kanal Ø
176504	XCSR	304	
176506	XBUF		
176510	RCSR	310	
176512	RBUF		Kanal 1
176514	XCSR	314	
176516	XBUF		
176520	RCSR	320	
176522	RBUF		Kanal 2
176524	XCSR	324	
176526	XBUF		
176560	RCSR	60	
176562	RBUF		Kanal 3
176564	XCSR	64	
176566	XBUF		

Bild 3

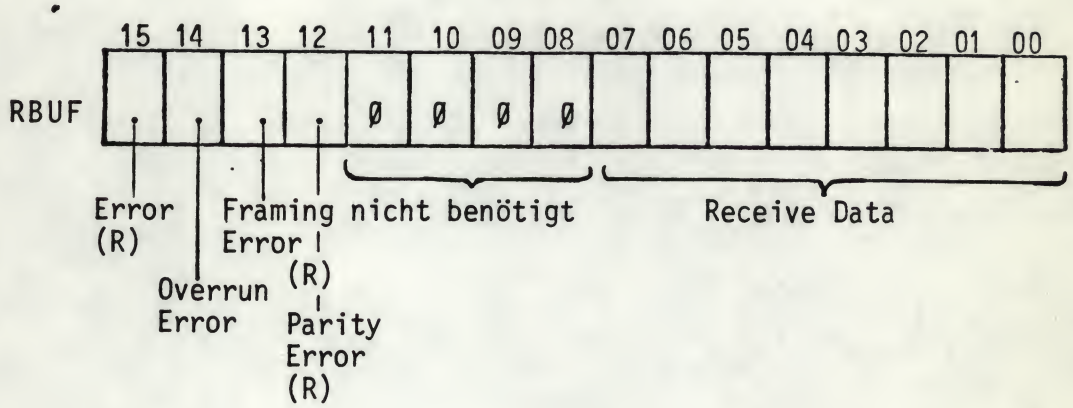
Es gibt 4 Wortformate, eines für jedes Device-Register innerhalb eines Kanals, die im folgenden beschrieben sind.

Receive Control/Status-Register



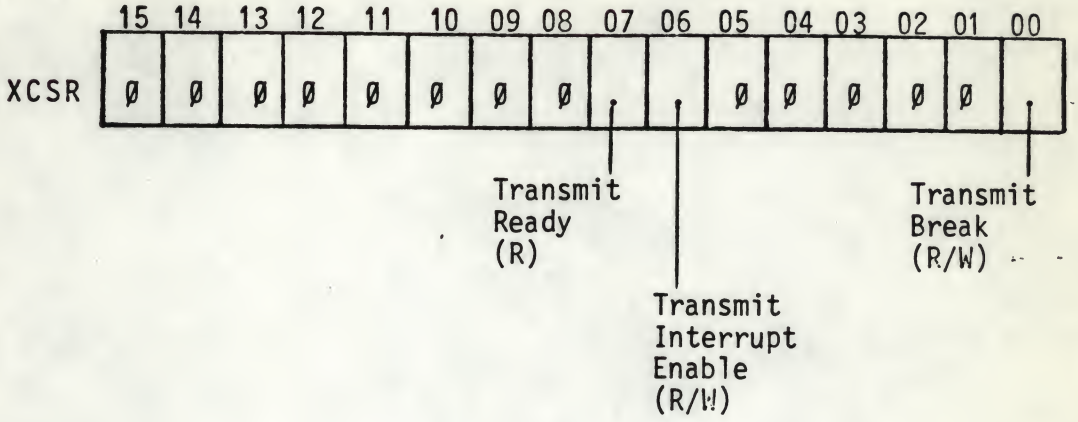
Bit	Beschreibung
8/15	Nicht benötigt. Beim Schreiben = Ø
7	Receiver Done. Wird gesetzt, wenn ein vollständiges Zeichen empfangen wurde und für die Eingabe in den Prozessor bereit ist. Das Bit wird automatisch gelöscht, wenn RBUF gelesen wird, BINITL angelegt wird oder das Bit Reader Enable gesetzt ist. Read Only Bit. Wenn das Bit 6 des RCSR gesetzt ist, bewirkt das Setzen des Bits 7 den Einsprung in eine Interrupt-Sequenz.
6	Receiver Interrupt Enable. Wird unter Programmkontrolle im Falle einer Receiver Interrupt Anforderung gesetzt (wenn ein Zeichen zur Übertragung in den Prozessor bereit ist). Wird gelöscht durch das Programm oder durch BINIT. Read/Write Bit.
1-5	Nicht benötigt. Beim Lesen = Ø
Ø	Reader Enable. Indem man dieses Bit setzt, geht der Lochstreifenleser am LT33-Terminal um ein Zeichen weiter. Durch das Setzen wird das Done-Bit (Bit 7) gelöscht. Write Only Bit. Die Benutzung dieses Bits setzt das Vorhandensein der DLV11-KA-Option voraus.

Receive Buffer



Bit	Beschreibung
15	Channel Error Status. Logisches 'OR' aus Bit 14,13 und 12. Read Only Bit.
14	Overrun Error. Wenn dieses Bit gesetzt ist, wird angezeigt, daß das Lesen eines Datums vor dem Senden eines neuen nicht beendet wurde. Wird durch BINIT gelöscht. Read Only Bit.
13	Framing Error. Das gesetzte Bit zeigt beim gelesenen Zeichen ein ungültiges Stop-Bit an. Wird durch BINIT gelöscht. Read Only Bit.
12	Parity Error. Die empfangene Parität stimmt nicht mit der erwarteten überein, wenn dieses Bit gesetzt ist. Falls das Device ohne Parität betrieben wird, ist dieses Read Only Bit immer Ø.
8-11	Nicht benötigt. Beim Lesen = Ø
Ø-7	Daten-Bits. Enthält 7 oder 8 Bits rechtsbündig. Read Only Bits.

Transmit Control/Status-Register



Bit	Beschreibung
8-15	Nicht benötigt. Beim Lesen = Ø
7	Transmit Ready. Wird gesetzt, wenn XBUF leer ist und ein neues Zeichen übertragen werden kann. Es wird ebenfalls durch INIT während einer Power-Up-Sequenz oder während einer Reset-Instruction gesetzt. Read Only Bit. Wenn das Transmitter Interrupt Enable Bit (Bit 6) gesetzt ist, bewirkt das Setzen des Transmit Ready Bits eine Interrupt-Sequenz.
6	Transmit Interrupt Enable. Wenn es erforderlich wird, eine Transmit Interupt Anforderung zu generieren, wird dieses Bit unter Programmkontrolle gesetzt. Während Power-Up oder Init-Function wird dieses Bit gelöscht. Read/Write Bit.
1-5	Nicht benötigt. Beim Lesen = Ø
Ø	Transmit Break. Wird unter Programmkontrolle gesetzt oder gelöscht. Wenn es gesetzt ist, wird eine zusammenhängende Leerzeichenkette übertragen. Transmit Done und Transmit Interrupt können jedoch weiter benutzt werden. Im gelöschten Zustand kann eine normale Zeichenübertragung stattfinden. Wird durch BINIT gelöscht. Read/Write Bit.

Einstellungen

Das folgende Kapitel beschreibt, wie der Anwender das Modul entsprechend seinem System und seiner Anwendung einstellen kann. Register-Adressen, Vektor, Übertragungs- und Interface-Funktionen sind durch Brücken einstellbar. Die Standardadreß- und Vektoreinstellung enthält nachfolgende Tabelle, ebenso die der Brücken und deren Position.

Kanalunabhängige Brücken

Brücke	Bed	Stellung	Std	Anw	Brücke	Bed	Stellung	Std	Anw	Brücke	Bed	Stellung	Std.	Anw
A12	Basis-Adresse	X-0 / X-1	X		A6	Adr.	R / J	X		C1	Konsole auf	X-0 / X-1	X	
A11		X-0 / X-1	X		A5		X-0 / X-1	X		C2	CH3	X-0 / X-1	X	
A10		X-0 / X-1	X		V7	Basis-Vec	R / J	X		Break Reakt. CH3	Inh. Halt Boot	R / X-H / X-B	X	
A9		X-0 / X-1	X		V6		R / J	X						
A8		X-0 / X-1	X		V5		X-0 / X-1			R10	Impulsformung bei V24 je nach Baud-Rate (Tabelle)		120k	
A7		R / J	X		M	Konsole	R / J	X		R23			120k	

Std.-Adr. 177500 | Anw.-Adr.: | Std.-Vec 300 | Anw.-Vec.:

Einstellung je Kanal

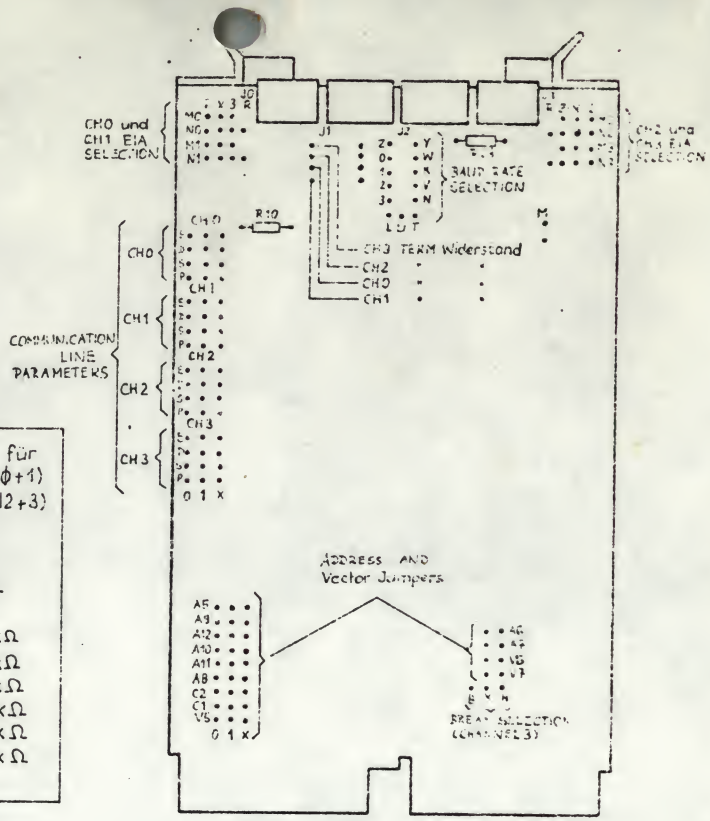
Brücke	Bedeutung	0 Stellung	0 Std	0 Anw	1 Stellung	1 Std	1 Anw	2 Stellung	2 Std	2 Anw	3 Stellung	3 Std.	3 Anw
Baud-rate	150 bd	0-U			1-U			2-U			3-U		
	300 bd	0-T			1-T			2-T			3-T		
	600 bd	0-V			1-V			2-V			3-V		
	1,2 kbd	0-W			1-W			2-W			3-W		
	2,4 kbd	0-Y			1-Y			2-Y			3-Y		
	4,8 kbd	0-L			1-L			2-L			3-L		
	9,6 kbd	0-N	X		1-N	X		2-N	X		3-N	X	
	19,2 kbd	0-K			1-K			2-K			3-K		
	38,4 kbd	0-Z			1-Z			2-Z			3-Z		
D	7 Datenbits	X-0			X-0			X-0			X-0		
	8 Datenbits	X-1	X		X-1	X		X-1	X		X-1	X	
S	1 Stop Bit	X-0			X-0			X-0			X-0		
	2 Stop Bits	X-1	X		X-1	X		X-1	X		X-1	X	
P	Parity enable	X-0			X-0			X-0			X-0		
	Parity inhibit	X-1	X		X-1	X		X-1	X		X-1	X	
E	Odd Parity	X-0			X-0			X-0			X-0		
	Even Parity	X-1	X		X-1	X		X-1	X		X-1	X	
M+N TERM M+N M	U-Norm EIA RS422	X-2			X-2			X-2			X-2		
		100Ω			100Ω			100Ω			100Ω		
	V24	X-3			X-3			X-3			X-3		
	20mA mit 900.611	X-3	X		X-3	X		X-3	X		X-3	X	
		X-R	X		X-R	X		X-R	X		X-R	X	

Tabelle für R10 (CH0+1) R23 (CH2+3)

1MΩ	
820 kΩ	
430 kΩ	
200 kΩ	
120 kΩ	
51 kΩ	
22 kΩ	

R = entfernt

J = eingesetzt



Standard Bildschirm-Terminal Baugruppe Anwendung

Einstell - Tabelle für DLV 11 - J (M8043)

3 900 610 3

UART-Funktionen

Die Funktion des UARTs (universeller asynchroner Empfänger und Sender) werden durch die Brücken D, S, P und E eingestellt - gemäß folgender Tabelle.

Bezeichnung	Kanal Parameter	X ZU Ø	X ZU 1	Bemerkungen
D	Nr. Datenbits	7	8	LSB zuerst übertragen
S	Nr. Stopbits	1	2	
P	Parität	Parität	keine	
E	gerade Parität	Ungerade erwartet	Gerade erwartet	Nur wenn P = Ø

Die Baud-Rate wird folgendermaßen eingestellt.

Bezeichnung	Baud-Rate	Brücke
U	150	nach Ø, 1, 2, 3 (Ø, 1, 2, 3 = Kanäle)
T	300	"
V	600	"
W	1 200	"
Y	2 400	"
L	4 800	"
N	9 600	"
K	19 200	"
Z	38 400	"

Zur Einstellung der Signalform bei den verschiedenen Baud-Raten sind folgende Widerstände nötig:

38,4 KB	22 K	
19,2 KB	51 K	
9,6 KB	120 K	
4,8 KB	200 K	
2,4 KB	430 K	R10 für CHØ und CH1
1,2 KB	820 K	
600 KB	1 M	R23 für CH2 und CH3
300 KB	1 M	
150 KB	1 M	
110 KB	1 M	

Bei Benutzung des Kanals 3 als Konsolenkanal läßt sich ein 'Break' folgendermaßen verarbeiten:

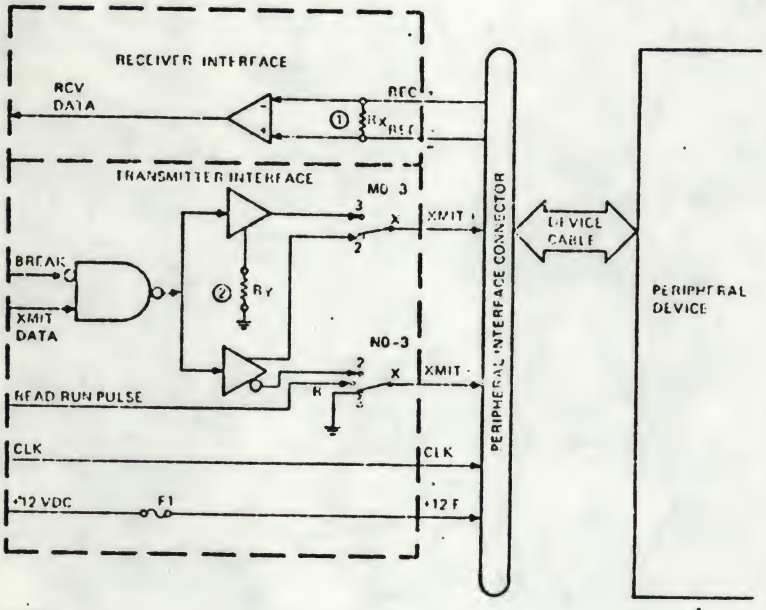
Boot	Brücke X nach B
Halt	Brücke X nach H
keine Antwort	keine Brücke

Schnittstellenfunktionen

Die Art der seriellen Schnittstelle wird durch die folgende Tabelle bestimmt:

Brücke	EIA RS-422	EIA RS-232C, RS-423	20mA Stromschleife mit DLV11-KA
MØ-3	X nach 2	X nach 3	X nach 3
NØ-3	X nach 2	X nach 3	X nach R
Anschluß Widerstand (einer pro Kanal)	100 1/4W		
Signalformung (einer pro Paar)		nach obiger Tabelle	
Fuse 1			1,0 A Pico Fuse

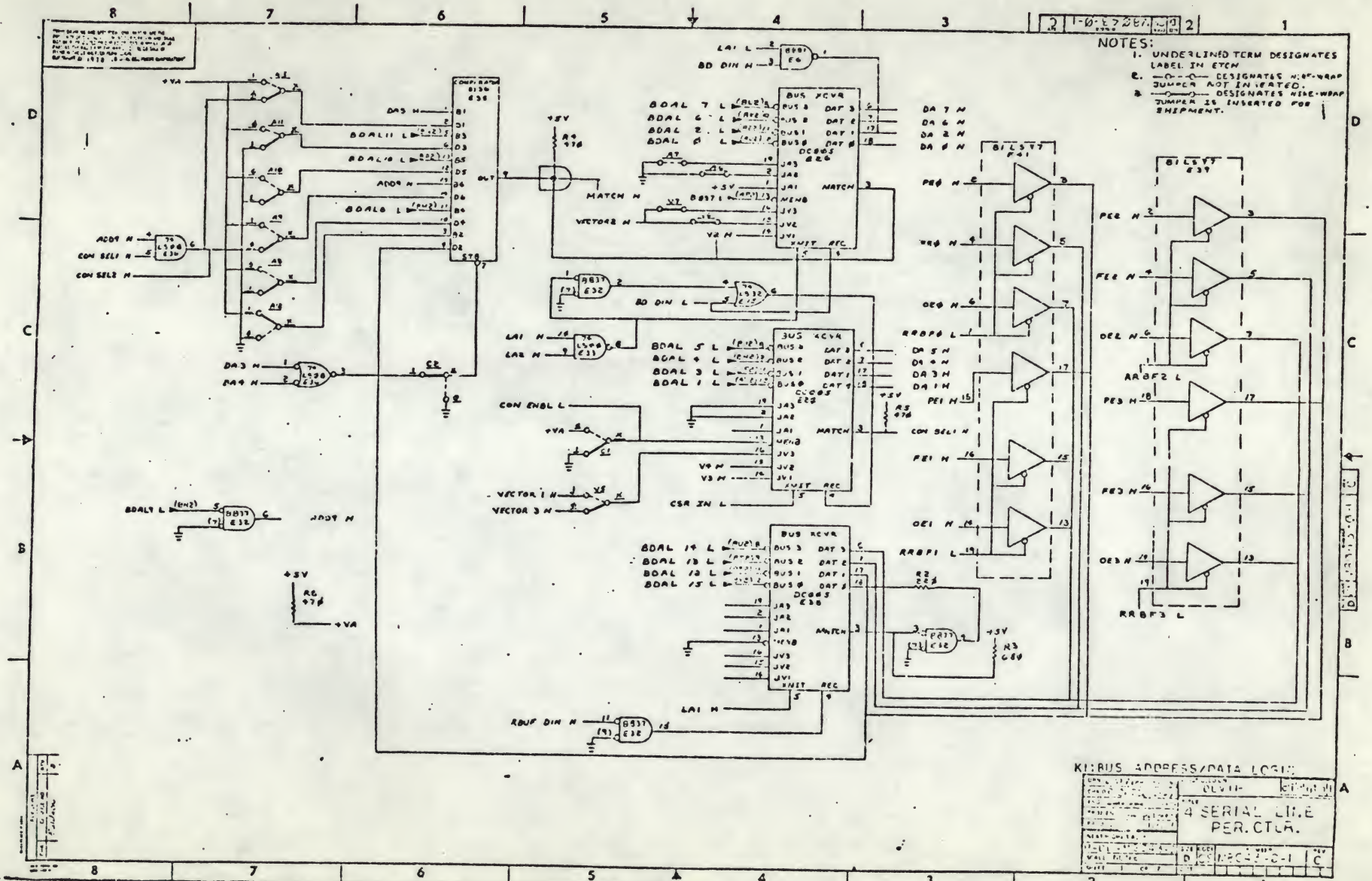
Bild 4 zeigt das Schlatbild eines typischen Interfaces.

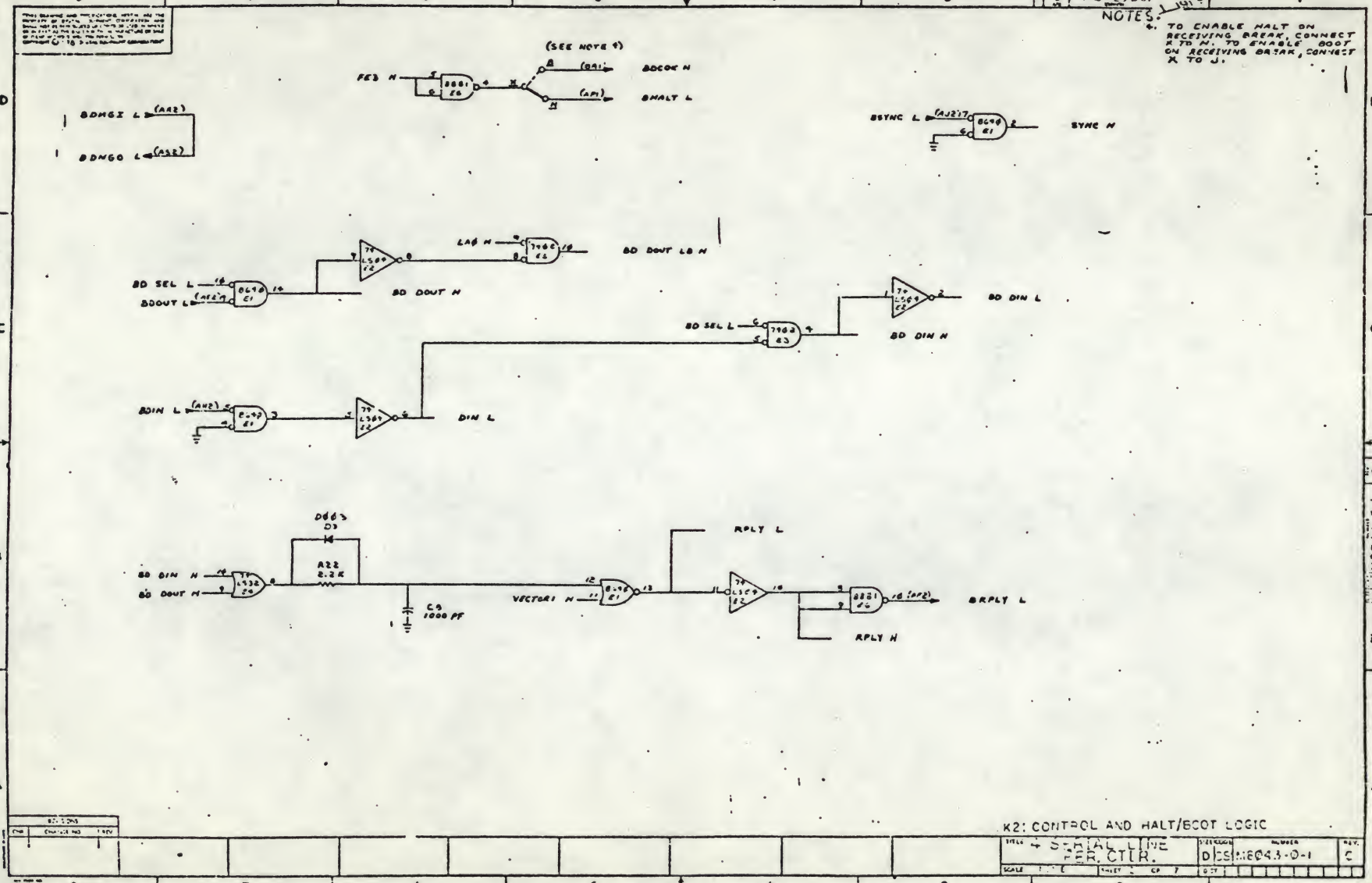


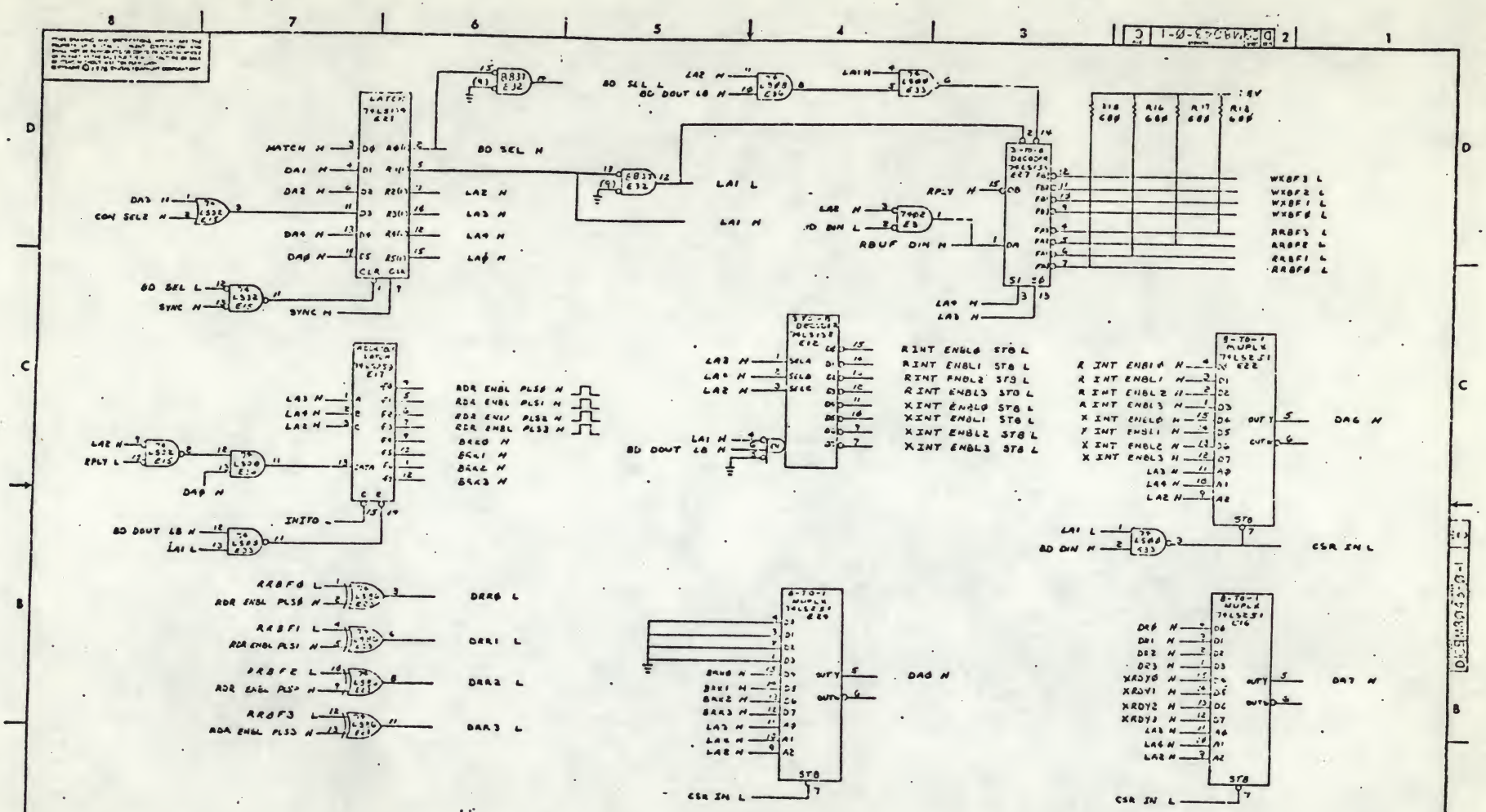
NOTES

① Rx IS INSTALLED WHEN CHANNEL IS CONFIGURED FOR EIA RS 422 OPERATION (100 Ω, 1/4 W NON WIRE WOUND)
R30 - CHANNEL 0
R31 - CHANNEL 1
R32 - CHANNEL 2
R33 - CHANNEL 3

② Ry IS CHOSEN FOR PROPER SLEW RATE WHEN CHANNEL IS CONFIGURED FOR EIA RS 232C/RS 423 OPERATION
R10 SETS SLEW RATE FOR CHANNELS 0 AND 1
R23 SETS SLEW RATE FOR CHANNELS 2 AND 3

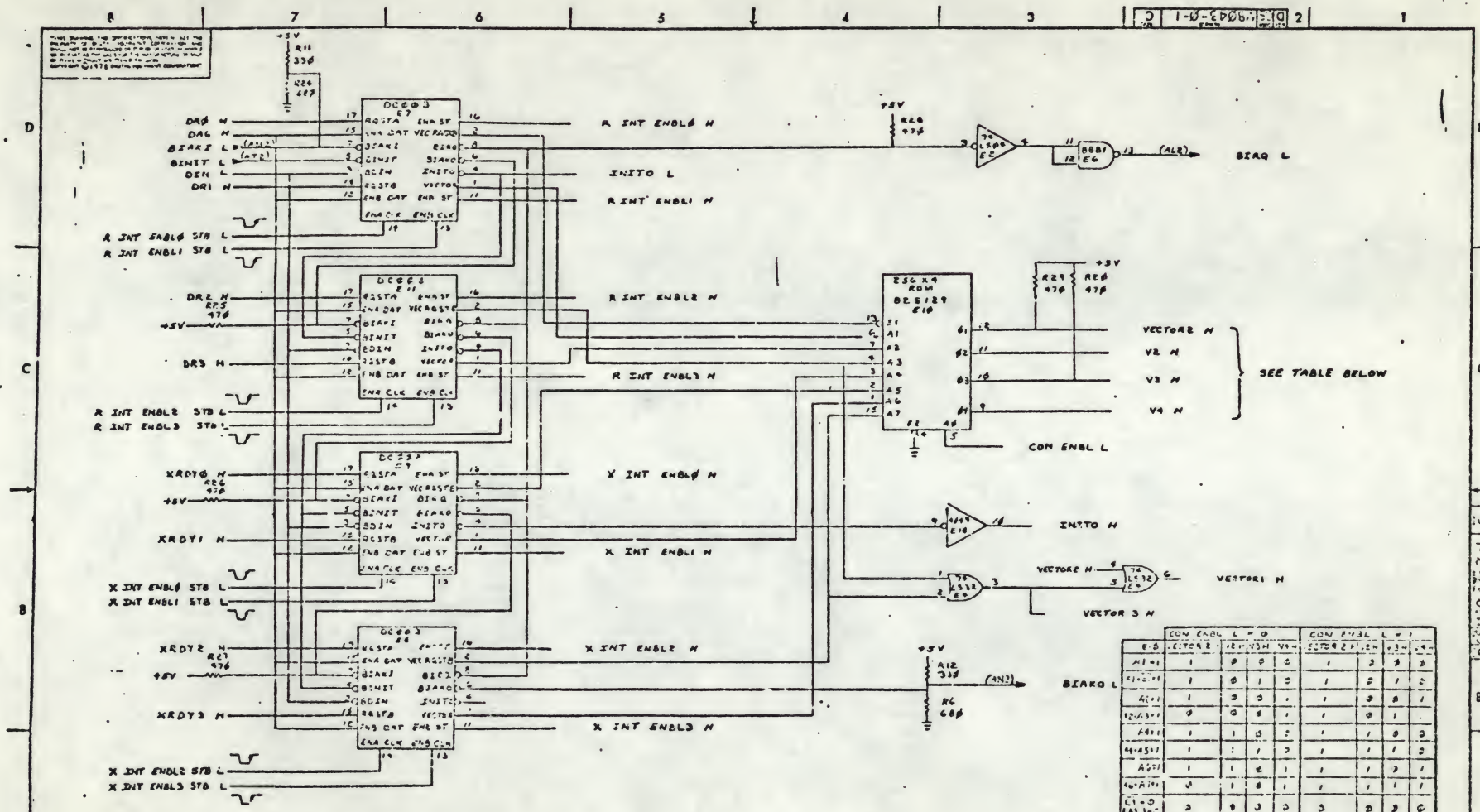

NOTES:
1. UNDERLINED TERM DESIGNATES LABEL IN ETCH
2. —o— DESIGNATES N.C.-WRAP JUMPER NOT INSERTED.
3. —o— DESIGNATES WIRE-WRAP JUMPER IS INSERTED FOR SHIPMENT.
KI:BUS ADDRESS/DATA LOGIC
4 SERIAL LINE PER. CTLR.


NOTES.
1. TO ENABLE HALT ON RECEIVING BREAK, CONNECT K TO N. TO ENABLE BOOT ON RECEIVING BREAK, CONNECT K TO J.
(SEE NOTE 1)
FE3 H
BDCOK H
BHALT L
BDMGI L
BDMGO L
BSYNC L
SYNC H
BD SEL L
BDOUT L
BD DOUT H
LA6 H
BD DOUT LB H
BD DIN L
BD DIN H
BDIN L
DIN L
D66
D3
A22
2.2K
C9
1000 PF
BD DIN H
BD DOUT H
VECTOR1 H
RPLY L
BRPLY L
RPLY H
K2: CONTROL AND HALT/BOOT LOGIC
4 SERIAL LINE PER. CTLR.
D-CS-8043-0-1
C



K3: ADDRESS LATCH AND REGISTER LOGIC

TITLE: 4 SERIAL LINE PER. CTLR.			
SCALE: NONE	SHEET 1 OF 7	DWG NUMBER: M5043-C-1	REV: C



	CON ENBL L = 0				CON ENBL L = 1			

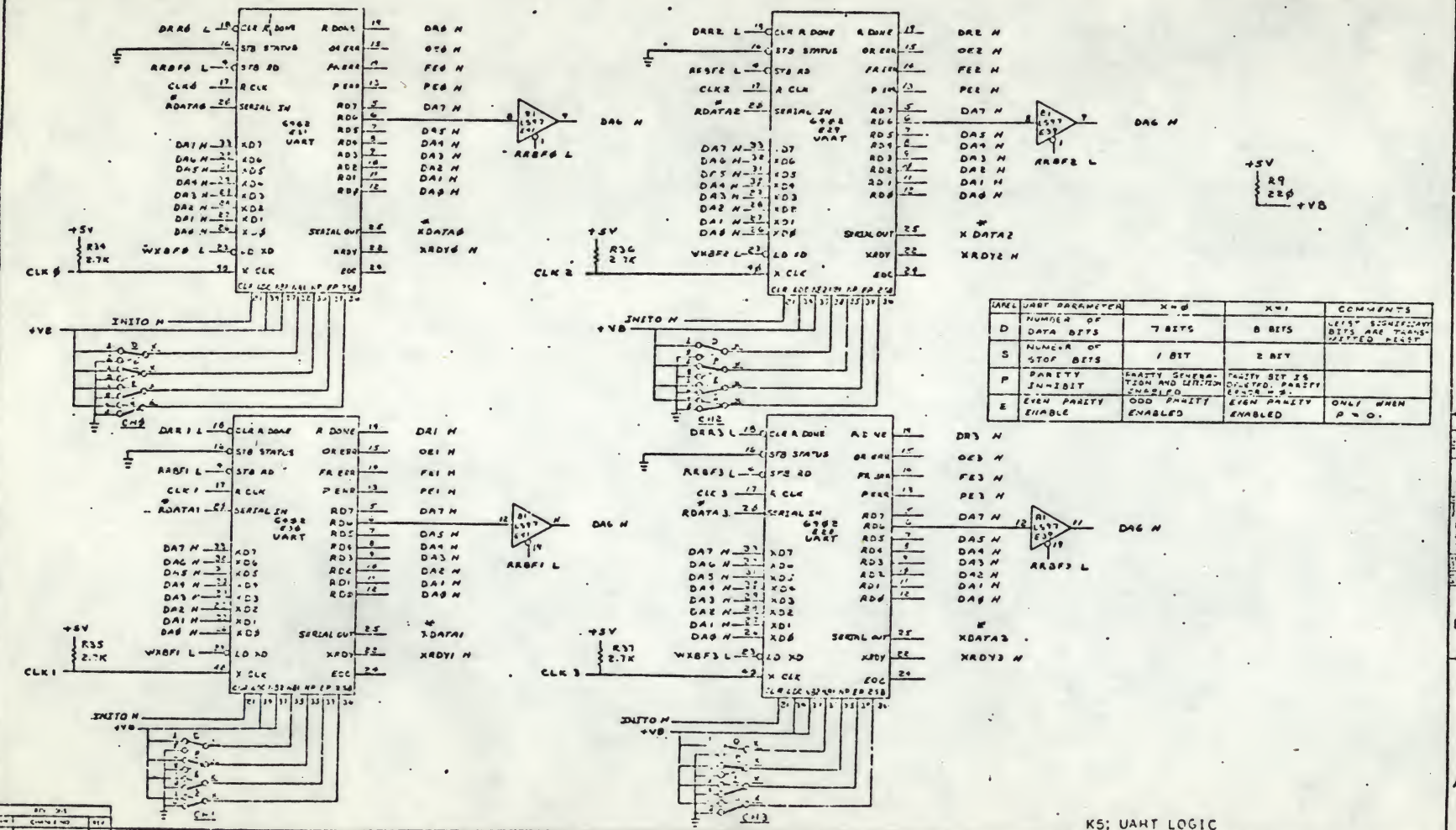
K4: INTERRUPT, VECTOR AND INIT LOGIC

4 SERIAL LINE BRK. CTLR.

DIS 1800-13-C-1

REV C

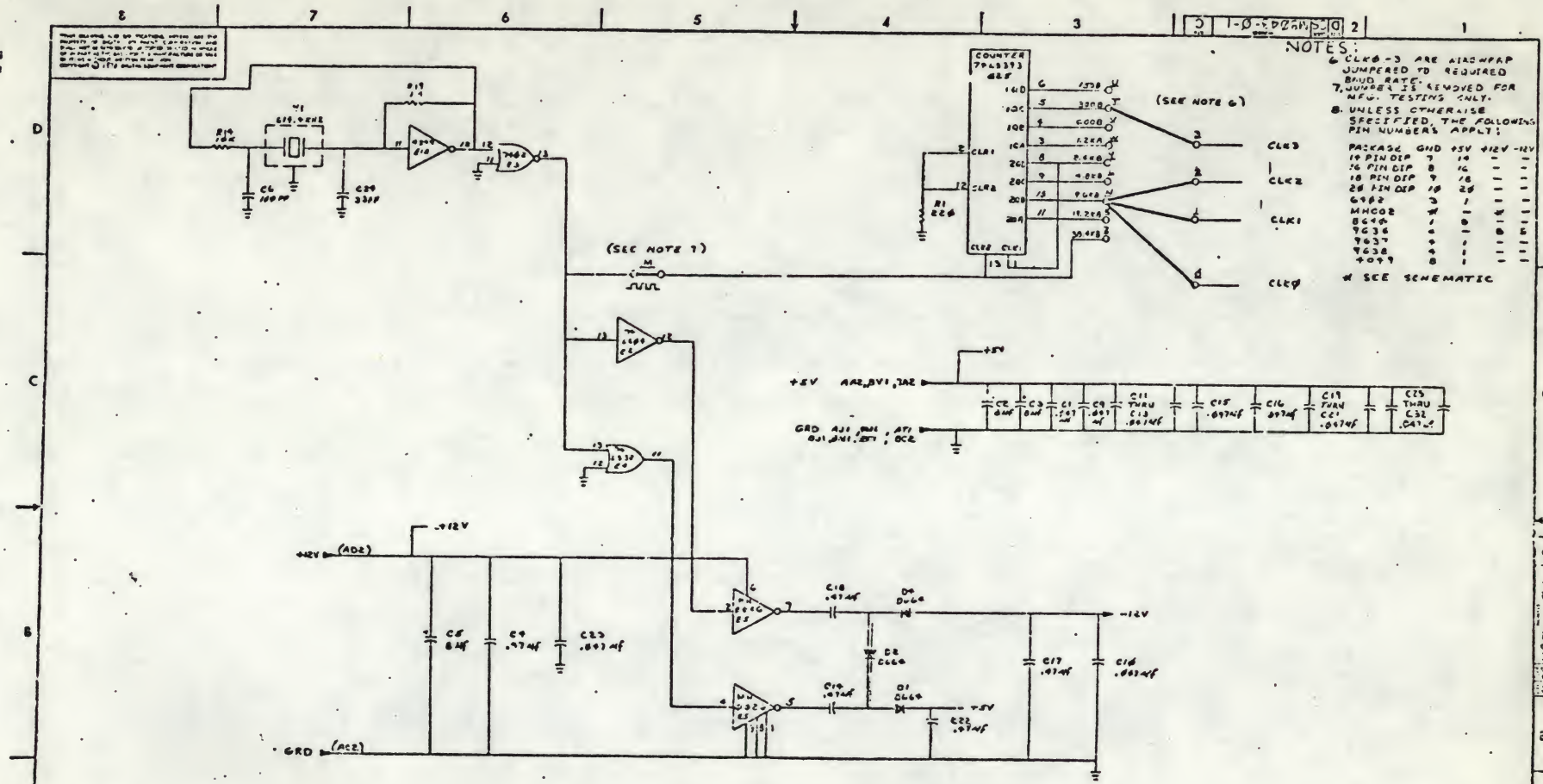
NOTES:
* 5. Y HIGH = MARK = 1
Y LOW = SPACE = 0

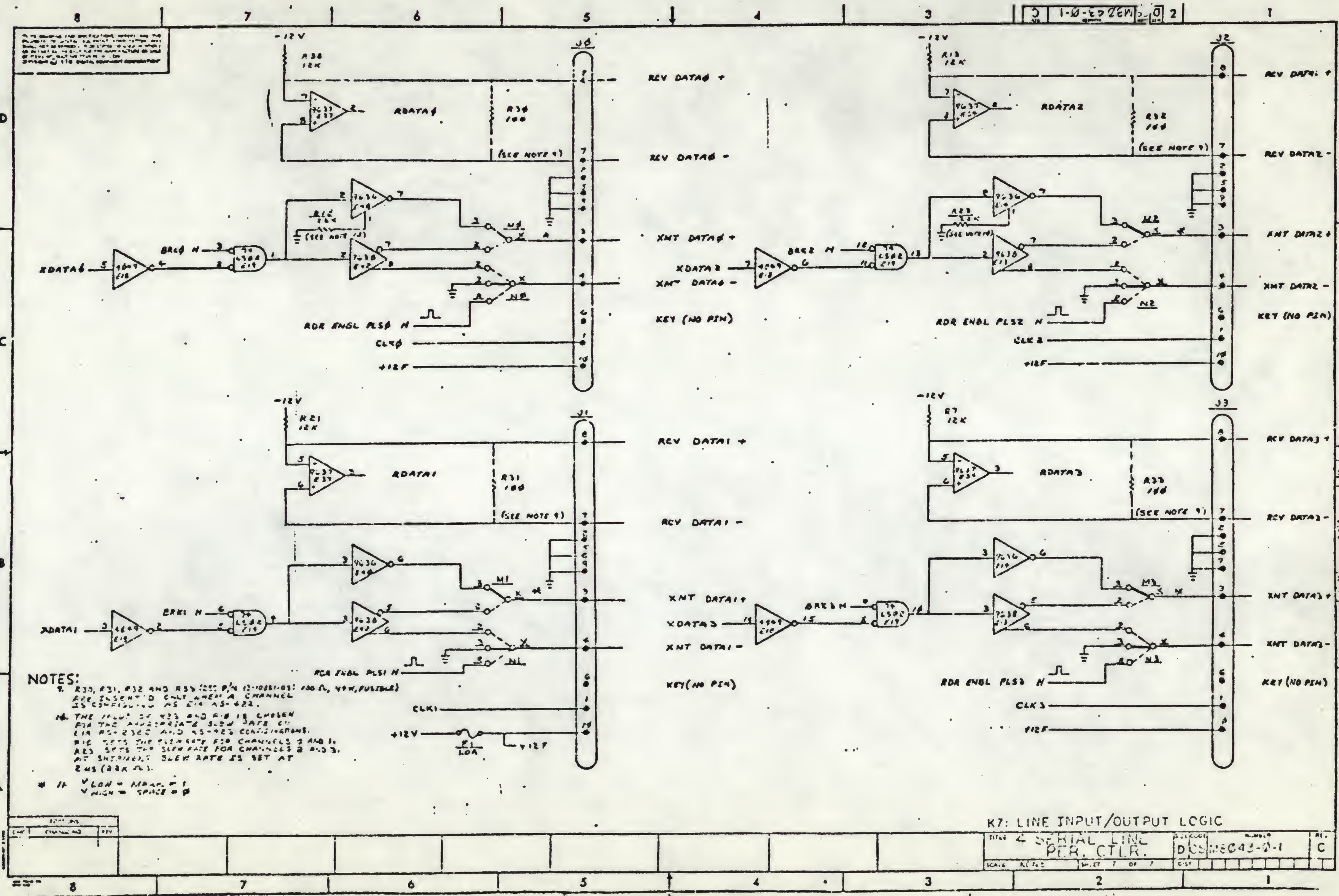


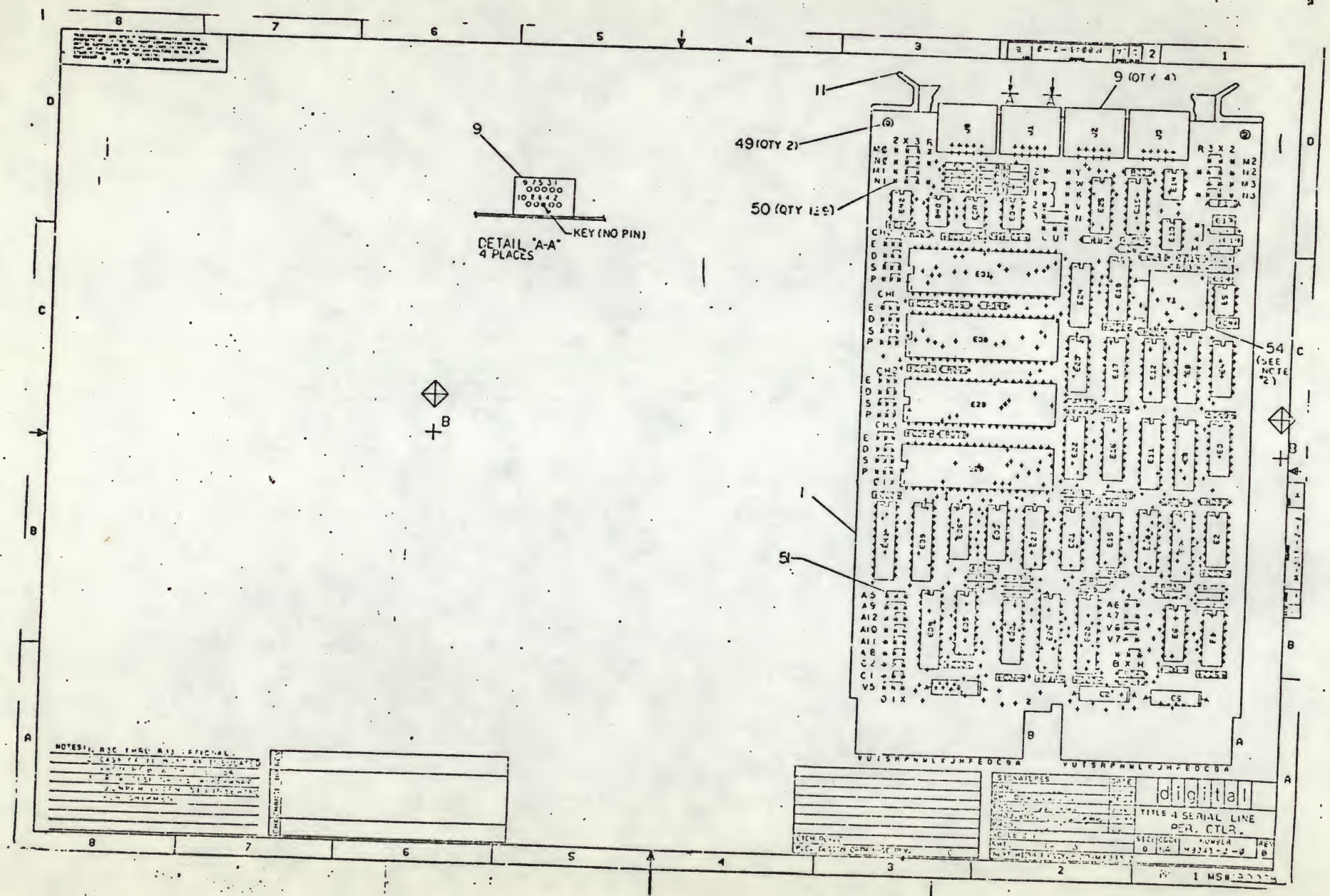
LABEL	UART PARAMETER	X=0	X=1	COMMENTS
D	NUMBER OF DATA BITS	7 BITS	8 BITS	LESS SIGNIFICANT BITS ARE TRANSMITTED FIRST
S	NUMBER OF STOP BITS	1 BIT	2 BIT	
P	PARITY IN=1 BIT	PARITY GENERATION AND VERIFICATION ENABLED	PARITY BIT IS DETECTED: PARITY ERROR = 1.	
E	EVEN PARITY ENABLE	ODD PARITY ENABLED	EVEN PARITY ENABLED	ONLY WHEN P = 0.

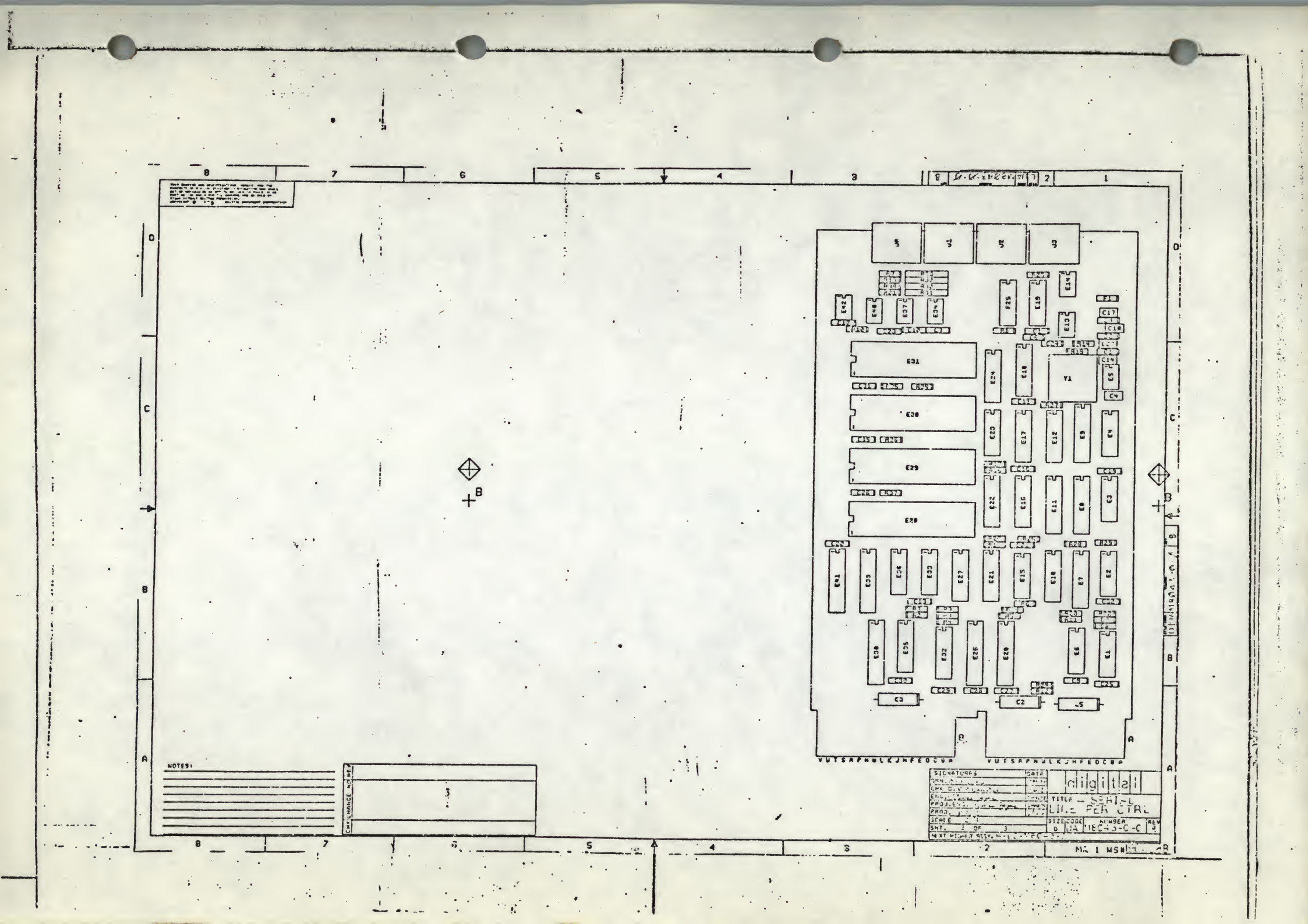
K5: UART LOGIC

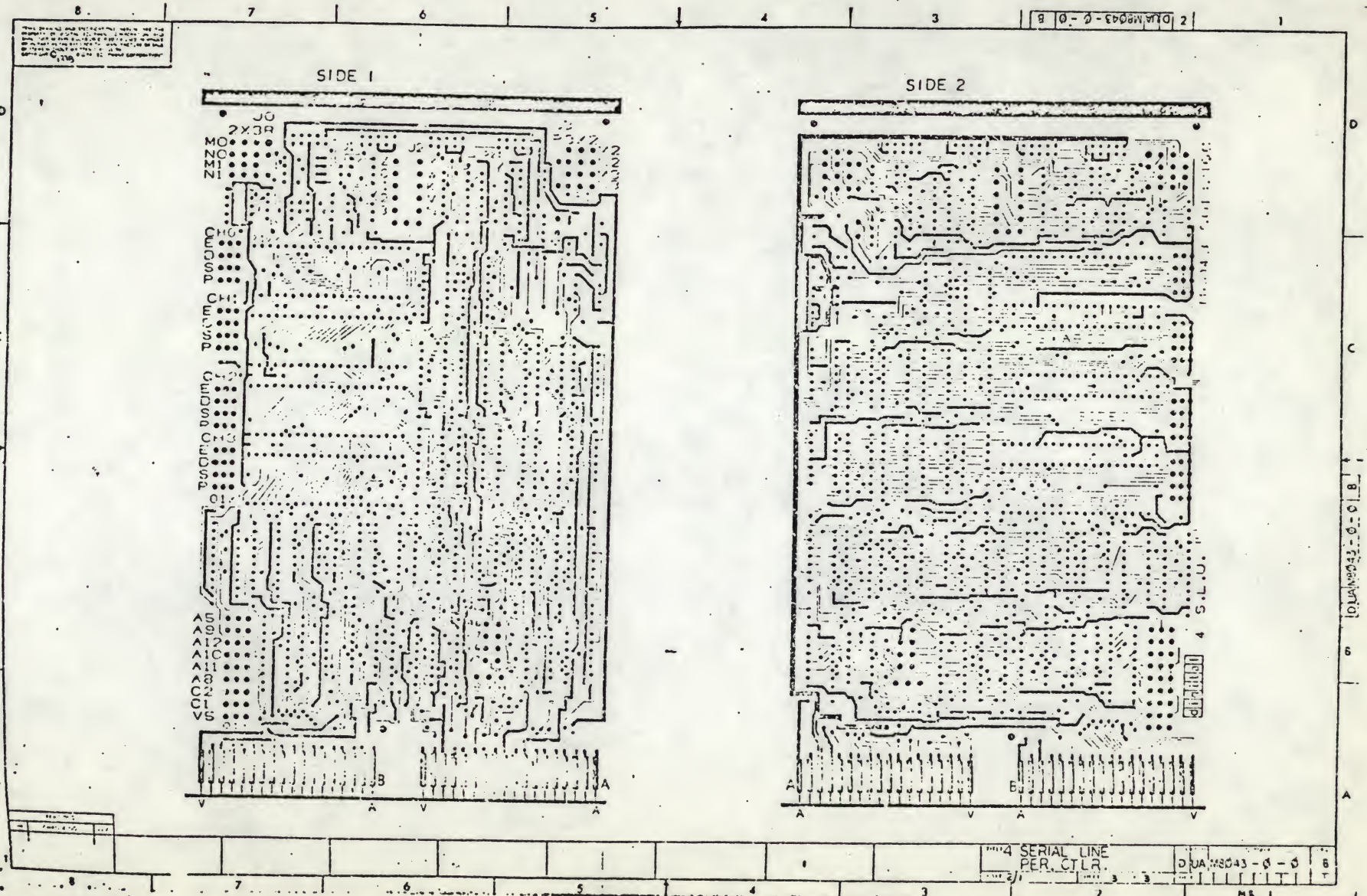
TITLE	SIZE	NUMBER	REV
4 SERIAL LINE PER. CTLR.	D	8043-0-1	C
SCALE: NONE	SHEET 5 OF 7		


NOTES:
6. CLK0-3 ARE AIRWRAP JUMPERED TO REQUIRED BAUD RATE.
7. JUMPER IS REMOVED FOR MFG. TESTING ONLY.
8. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:
PACKAGE GND +5V +12V -12V
14 PIN DIP 7 14 - -
16 PIN DIP 8 16 - -
18 PIN DIP 9 18 - -
24 PIN DIP 12 24 - -
6982 3 1 - -
MMC02 14 - - -
8644 1 8 - -
9636 4 1 - -
9637 4 1 - -
9638 4 1 - -
4049 8 1 - -
SEE SCHEMATIC
COUNTER 7040393
(SEE NOTE 6)
CLK3
CLK2
CLK1
CLK0
(SEE NOTE 7)
+5V
+12V (ADS)
-12V
GRD (ACC)
K6: PWR DIST, BAUD RATE GEN & -12V CIRCUITRY
4 SERIAL LINE PER. CTR.
DCS M8043-0-1
SCALE NONE
SHEET 6 OF 7
REV C


K7: LINE INPUT/OUTPUT LOGIC
4 SERIAL LINE PCR. CTLR.
D CS M8043-0-1
C
NOTES:
RCV DATA0 +
RCV DATA0 -
XNT DATA0 +
XNT DATA0 -
KEY (NO PIN)
RCV DATA1 +
RCV DATA1 -
XNT DATA1 +
XNT DATA1 -
KEY (NO PIN)
RCV DATA2 +
RCV DATA2 -
XNT DATA2 +
XNT DATA2 -
KEY (NO PIN)
RCV DATA3 +
RCV DATA3 -
XNT DATA3 +
XNT DATA3 -
KEY (NO PIN)
XDATA0
XDATA1
XDATA2
XDATA3
RDATA0
RDATA1
RDATA2
RDATA3
RDR ENBL PLS0 H
RDR ENBL PLS1 H
RDR ENBL PLS2 H
RDR ENBL PLS3 H
CLK0
CLK1
CLK2
CLK3
+12F
+12V
-12V
J0
J1
J2
J3
(SEE NOTE 9)


9
49 (QTY 2)
50 (QTY 12)
DETAIL "A-A"
4 PLACES
KEY (NO PIN)
11
9 (QTY 4)
54
(SEE NOTE 2)
1
51
digital
TITLE: SERIAL LINE
PER. CTLR.


NOTES:
digitsi
SERIAL LINE PCB CTRL
MECH-3-C-C


SIDE 1
SIDE 2
4 SERIAL LINE PER CTLR.
DUA W8043 - Ø - Ø

WIRE TABLE

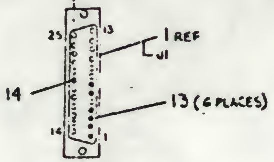
ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONN	FROM WITH	TO CONN	TO WITH	REMARKS
3	22	BLK	P1-2	ITEM 5	J1-7	ITEM 13	PAIR
3	22	RED	P1-3	ITEM 5	J1-2	ITEM 13	PAIR
3	22	DRAIN	—	ITEM 5 ENDS	J1-1 SEE NOTE 1	ITEM 13	PAIR
3	22	DRAIN	—	ITEM 5 ENDS	CUT SEE NOTE 2	—	PAIR
3	22	BLK	CUT	—	CUT	—	SEE NOTE 2
3	22	WHT	P1-8	ITEM 5	J1-3	ITEM 13	PAIR
3	22	BLK	CUT	—	CUT	—	SEE NOTE 2
3	22	GRN	P1-10	ITEM 5	—	—	SEE NOTE 3
3	22	DRAIN	CUT	—	CUT	—	SEE NOTE 2
7	22	YEL	P1-7	ITEM 5	P1-9	ITEM 5	2 IN LONG
7	22	YEL	J1-6	ITEM 13	J1-4	ITEM 13	2 IN LONG

LEGEND

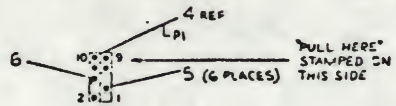
NUMBER	DIM 'X' VAR.	DIM 'Y' PRECUT VAR.
BC21B-05	5 FT 0 IN	5 FT 2 IN

NOTES:

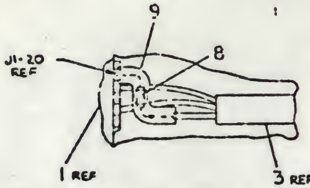
1. DRAIN WIRES TO BE ENCLOSED WITH ITEM 8 FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER CONTACT OR TERMINAL.
2. MYLAR SHIELDS AND SPECIFIED WIRES ARE CUT FLUSH WITH JACKET.
3. AT J1 END, WIRE FROM P1-10 (GRN) IS SOLDERED TO ITEM 8. OTHER END OF ITEM 9 IS SOLDERED TO ITEM 14, ITEM 9 PUT ON AND INSTALLED IN J1-20.



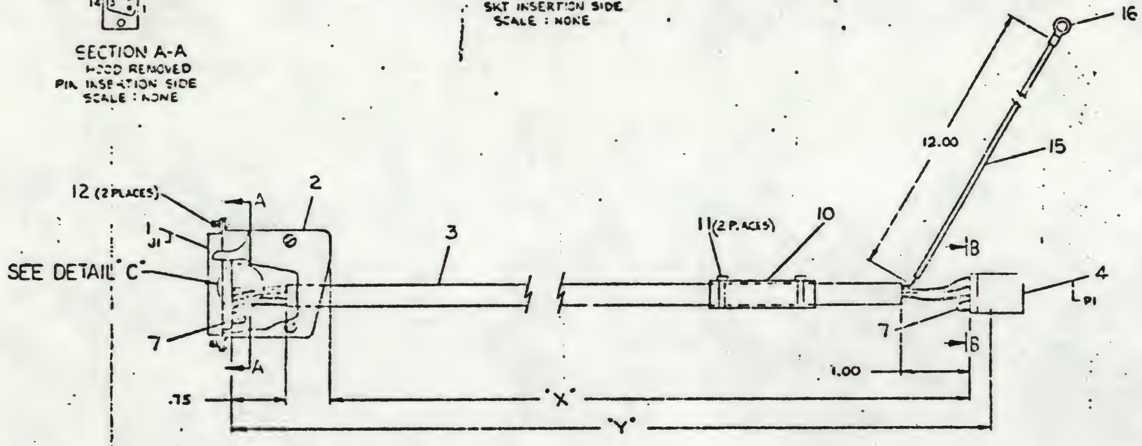
SECTION A-A
HOOD REMOVED
PIN INSERTION SIDE
SCALE : NONE



VIEW B-B
SKT INSERTION SIDE
SCALE : NONE



DETAIL 'C'
SCALE : NONE
SEE NOTE 3



PARTS LIST

QTY	DESCRIPTION	PART NO.	ITEM
1	TERMINAL, RING	9007930	16
A/R	TUBING, THIN EXTRUDED [illegible]	[illegible]	15
1	CONTACT, PIN	1210493-45	14
6	CONTACT, PIN	1210493-[illegible]	13
1	SCREW, RETAINER MALE	1210493-51	12
2	TIE WRAP	[illegible]	11
1	LABEL, CABLE IDENT	[illegible]	10
A/R	TUBING, HEAT SHRINK, CLR	9012[illegible]3-[illegible]	9
1	RESISTOR, 150Ω, 5% [illegible] W	[illegible]	8
A/R	WIRE, 22 AWG STRANDED [illegible]	[illegible]-44	7
1	PLUG, KEYING	12154[illegible]5-00	6
6	CONTACT, SOCKET	1214[illegible]	5
1	TERMINATOR, HOUSING	1214[illegible]	4
A/R	CABLE, 3PR, SHIELDED	9 [illegible]7725	3
1	HOOD & STRAIN RELIEF	1210493-50	2
1	SHELL & INSERT	[illegible]	1

CABLE, MODEM
ASSY.

SIZE D
MATERIAL SEE PARTS LIST

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE DLVII-F ENGINEERING SPECIFICATION

10.0 ENVIRONMENTAL REQUIREMENTS

10.1 Ambient Temp

Operating	5°C to 60°C (41°F to 140°F)
Non-Operating	-40°C to 80°C (-40°F to 176°F)

10.2 Humidity

Operating	10% to 95%, Max wet bulb 32°C (90°F) and Min dew point 2°C (36°F)
Non-Operating	5% to 95%

10.3 Altitude

Operating	2.4km (8,000 ft)
Non-Operating	9.1km (30,000 ft)

SIZE	CODE	NUMBER	REV
A			

SHEET 25 OF 25

contains a crystal oscillator which is connected to a dual baud rate generator which provides appropriate clock signals to the UART. A separate clock is available for the transmitter for split speed operation.

8.2.7 -12V Charge Pump

This circuit provides the -12 volts needed by the UART, the driver (1488) and the FOR RUN current loop. The maximum current supplied by this -12V charge pump is 40mA.

8.2.8 Reader Run Circuit

The Reader Run Circuit is used to advance the pape. tape reader in the DEC modified TTY units. This is performed by setting bit 5 of the RCSR to a 1. The Reader Run Circuit then will advance the paper tape one position and serial data will start to be received from the TTY. The start bit of this serial data is used by the Reader Run Circuit to automatically reset the internal bit 5 flip-flop.

8.2.9 20mA Interface

This circuit converts TTL level serial data to standard 20mA Current Loop Serial Data and vice versa. This circuit allows direct connection to DECwriter LA36, VT52, etc. and to the DEC modified TTY. Both the receiver and transmitter may operate in either the active or passive mode.

8.2.10 EIA Interface

This interface provides the proper level converters for serial data for connection to EIA terminals such as the VT06 or the model 37 TTY through a null modem. (See EIA standard RS-232-C).

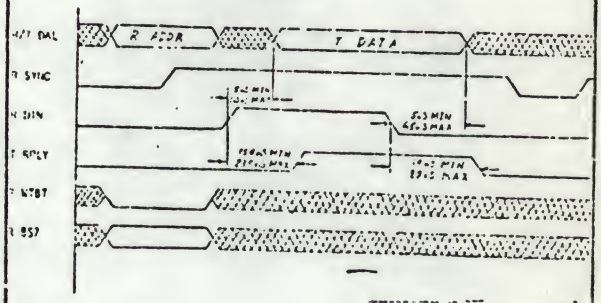
This circuit straps EIA Data Terminal Ready, EIA Request to Send signals to the ON position, thus making it possible for the DLV11-F to interface to the Model 103A2 datasets which will automatically answer incoming calls. This type of connection, however, does not provide for properly terminating the call.

EIA FORCE BUSY signal is also strapped ON for use with the model 103E modems.

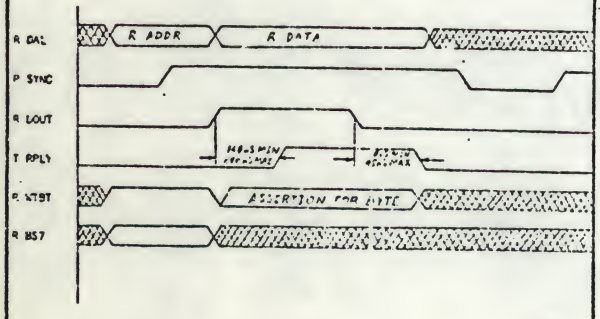
9.0 TIMING DIAGRAMS

In the following timing diagrams, signals are referenced from the output of the bus receiver to the input of the bus driver.

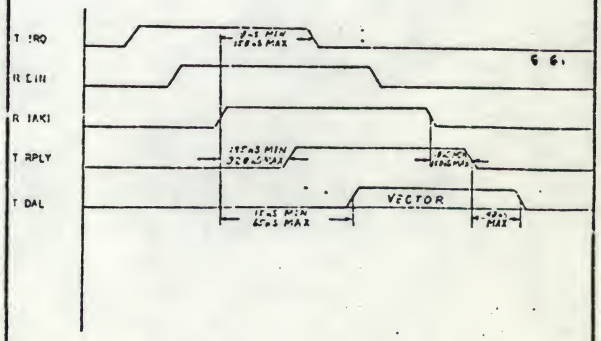
9.1 DAT Bus Cycle Timing



9.2 DATO or DATOB Bus Cycle



9.3 Interrupt Timing



Bit	Name	Meaning and Operation
1	RESERVED	Not applicable. Read as 0s.
0	BREAK	When set, transmits a continuous space to the external device. Read/write bit cleared by INIT.

7.1.4 Transmitter Buffer Register

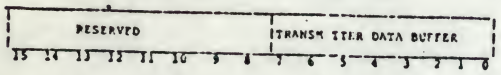


FIGURE 5 TRANSMITTER BUFFER REGISTER (XBUF) - BIT ASSIGNMENTS

Bit	Name	Meaning and Operation
15-8	RESERVED	Not applicable. Undefined when read.
7-0	TRANSMITTER DATA BUFFER	Holds the character to be transferred to the external device. If less than eight bits are used, the character must be loaded so that it is right justified into the least significant bits. Write only bits. Undefined when read.

7.2 Interrupts

The DLV11-F has two interrupt channels: one for the receiver section and one for the transmitter section. These two channels operate independently; however, if simultaneous interrupt requests occur, the receiver has priority.

A transmitter interrupt can occur only if the interrupt enable bit (XMIT INT ENB) in the transmitter status register is set. With XMIT INT ENB set, setting the transmitter ready (XMIT RDY) bit initiates an interrupt request. When XMIT RDY is set, it indicates that the transmitter buffer is empty and ready to accept another character from the bus for transfer to the external device.

A receiver data interrupt can occur only if the interrupt enable (RCVR INT ENB) bit in the receiver status register is set. With RCVR INT ENB set, setting the receiver done (RCVR DONE) bit initiates an interrupt request. When RCVR DONE is set, it indicates that an entire character has been received and is ready for transfer to the bus.

7.3 Timing Considerations

When programming the DLV11-F Asynchronous Line Interface, it is important to consider timing of certain functions in order to use the system in the most efficient manner. Timing considerations for the receiver, transmitter and break generation logic are discussed in the following paragraphs.

7.3.1 Receiver

The RCVR DONE flag (bit 7 in the RCSR) sets when the Universal Asynchronous Receiver/Transmitter (UART) has assembled a full character. This occurs at the middle of the first STOP bit. Because the UART is double buffered, data remains valid until the next character is received and assembled. This permits one full character time for servicing the RCVR DONE flag.

7.3.2 Transmitter

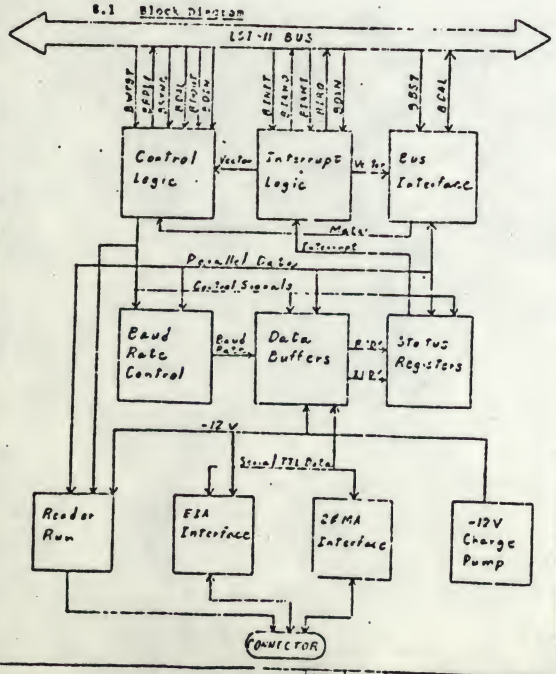
The transmitter section of the UART is also double buffered. The XMIT RDY flag (bit 7 in the XCSR) is set after initialization. When the buffer (XBUF) is loaded with the first character from the bus, the flag clears but then sets again within a fraction of a bit time. A second character can then be loaded, which clears the flag again. The flag then remains cleared for nearly one full character time.

7.3.3 Break Generation Logic

When the BREAK bit is set, it causes transmission of a continuous space. Because the XMIT RDY flag is set after transmission of a character, the duration of a break can be timed by the pseudo-transmission of a number of characters. Therefore, because the transmitter section of the UART is double buffered, a null character (all 0s) should precede transmission of the break to ensure that the previous character clears the line. In a similar manner, the final pseudo-transmitted character in the break should be a null.

8.0 LOGIC DESCRIPTION

8.1 Block Diagram



8.2 Logic Discussion

8.2.1 Bus Interface

The bus interface is comprised partly of DC895 transceiver chips. These chips contain bus transceivers that connect the BDAL lines with the internal tri-state bidirectional bus. This chip also provides jumper inputs for address selection and asserts a MATCH H open collector output signal when there is an address match. These chips also contain jumper inputs for vector address selection that allow the vector to be asserted on the BDAL lines of the bus.

8.2.2 Interrupt Logic

The interrupt logic provides for two interrupts, A and B, with A having the highest priority. Part A services the receiver interrupts and Part B services the transmitter interrupts.

8.2.3 Control Logic

The major portion of the control logic is provided by the DC294 protocol chip. The protocol chip receives DSYNC, DOUT, DSYNC, DWTBT and issues DRPLY. It also generates outputs based on the three least significant BDAL lines indicating which of the on-board registers are being addressed. It also indicates which byte or bytes are being operated on and whether the transaction is a DIN or, DOUT.

8.2.4 Status Registers

There are two status registers on the module, a receiver status register and a transmitter status register. Information is fed to the flip-flops comprising the status registers via the tri-state DAT bus, information is read from the registers also through this same DAT bus.

8.2.5 Data Buffers

The data buffers are comprised of a Universal Asynchronous Receiver/Transmitter (UART). The UART accepts parallel data and serializes it with start bits and stop bits for transmitter operations. It also accepts serial data and changes it in parallel form for receiver operations.

8.2.6 Baud Rate Control

The baud rate is jumper selectable or program selectable over the range 50 - 19200 baud. The circuit

7.0 PROGRAMMING SPECIFICATION

All software control of the DLV11-F Asynchronous Line Interface is performed by means of four device registers. These registers are in sequential addresses and can be read or loaded (with the exceptions noted) using any LSI-11 instruction referring to their addresses.

Figures 2 through 5 show the bit assignments for the four device registers.

The reserved and write only bits are always read as 0s* (with the exception of the Transmitter Buffer Register). Loading reserved or read only bits has no effect on the bit position. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by issuing a programmed RESET instruction or the occurrence of a power-up or power-down condition of the processor power supply.

In the following descriptions, "transmitter" refers to those registers and bits involved in accepting a parallel character from the LSI-11 Bus for serial transmission to the external device; "receiver" refers to those registers and bits involved with receiving serial information from the external device for parallel transfer to the LSI-11 Bus.

7.1 Device Registers

7.1.1 Receiver Status Register

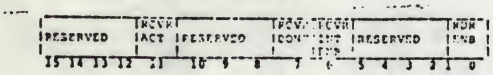


FIGURE 2 RECEIVER STATUS REGISTER (RCSR) - BIT ASSIGNMENTS

Bit	Name	Meaning and Operation
15-12	RESERVED	Not applicable. Read as 0s.
11	RCVR ACT (Receiver Active)	When set, this bit indicates that the DLV11-F interface receiver is active. The bit is set at the center of the START bit which is the beginning of the input serial data from the device and is cleared by the leading edge of RCVR DONE.

*Bits in the Transmitter Buffer are undefined when used.

Bit	Name	Meaning and Operation
		Read only bits cleared by INIT.
10-8	RESERVED	Not applicable. Read as 0s.
7	RCVR DONE (Receiver Done)	This bit is set when an entire character has been received and is ready for transfer to the LSI-11 Bus. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 6) is also set. Cleared whenever the receiver buffer (RBUF) is addressed or whenever RDR ENB (bit 0) is set. Read only bit. Cleared by INIT.
6	RCVR INT ENB (Receiver Interrupt Enable)	When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets. Read/write bit; cleared by INIT.
5-1	RESERVED	Not applicable. Read as 0s.
0	RDR ENB (Reader Enable)	When set, this bit advances the paper tape reader in DEC modified TTY units and clears the RCVR DONE bit (bit 7). This bit is cleared at the middle of a START bit which is the beginning of the serial input from an external device. Also cleared by INIT. Write only bit.

7.1.2 Receiver Buffer Register

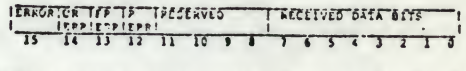


FIGURE 3 RECEIVER BUFFER REGISTER (RBUF) - BIT ASSIGNMENTS *

Bit	Name	Meaning and Operation
15	ERROR	Used to indicate that an error condition is present. This bit is the logical OR

Bit	Name	Meaning and Operation
		of CR ERR, FR ERR and P ERR (bits 14, 13, and 12 respectively). Whenever one of these bits is set, it causes ERROR to set. This bit is not connected to the interrupt logic. Read only bit, cleared by removing the error producing condition. Cleared by INIT.
	NOTE:	ERROR indications remain present until the next character is received, at which time the error bits are updated.
14	CR ERR (Overrun Error)	When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read only bit. Cleared by INIT.
13	FR ERR (Framing Error)	When set, indicates that the character that was read had no valid STOP bit. Read only bit. Cleared by INIT.
12	P ERR (Parity Error)	When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected. Read only bit. Cleared by INIT.
11-8	RESERVED	Not applicable. Read as 0s.
7-0	RECEIVED DATA BITS	Holds the character just read. If less than eight bits are selected, then the buffer is right justified into the least significant bit positions. In this case, the higher unused bit or bits read as 0s. Read only bits, not cleared by INIT.

7.1.3 Transmitter Status Register

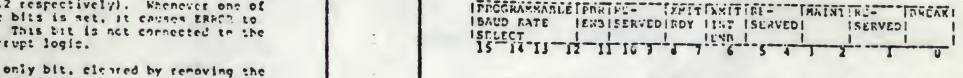


FIGURE 4 TRANSMITTER STATUS REGISTER (XCSR) - BIT ASSIGNMENTS

Bit	Name	Meaning and Operation
15-12	PBR SEL (Programmable Baud Rate Select)	When set, these bits choose a baud rate from 50 - 19200 baud. See TABLE 1. Write only bits; read as 0s. Not cleared by INIT.
11	PBR ENB (Programmable Baud Rate Enable)	This bit must be set in order to select a new baud rate indicated by bits 12 to 15. Write only bit; read as 0. Not a latched bit.
10-8	RESERVED	Not applicable, read as 0s.
7	XMIT RDY (Transmitter Ready)	This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT END (bit 6) is also set. Ready only bit. Set by INIT. Cleared by loading the transmitter buffer.
6	XMIT INT END (Transmitter Interrupt Enable)	When set, allows an interrupt sequence to start when XMIT RDY (bit 7) is set. Read/write bit; cleared by INIT.
5-3	RESERVED	Not applicable. Read as 0s.
2	MAINT (Maintenance)	Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed. Read/write bit; cleared by INIT.

6.0 CONFIGURATIONS

6.1 Jumper Definitions

Jumper	Definition
A3-A12	Jumpers inserted will provide a match with the corresponding Bus Address bit. Selectable from 160000 to 177777.
V3-VP	Jumper inserted will assert the corresponding Vector address bit on the LSI-11 Bus. Selectable from 000 to 774.
R0-R3	UART Receiver and Transmitter baud rate select jumpers during common mode of operation. UART Receiver only baud rate select jumpers during split speed. See Table 1.
T0-T3	UART Transmitter baud rate select jumpers during split speed operation and when the Maintenance Bit is set. See Table 1.
BG	Jumper inserted to enable Break Generation.
P	Jumper inserted for Parity generation by the UART. (Odd or even parity is selected by the -E jumper.)
-E	Jumper removed for Even parity and inserted for odd parity. (Receiver checks for appropriate parity and transmitter inserts the appropriate parity.)
1, 2	Selects desired number of data bits. (I = Inserted, R = Removed).

2	1	No. of Data Bits
I	I	5
I	R	6
R	I	7
R	R	8

C, C1	Jumpers inserted for Common speed operation on UART Receiver and Transmitter clocks. (Note that jumpers S and S1 must be removed.)
S, S1	Jumpers inserted for Split speed operation on UART Receiver and Transmitter clocks. (Note that jumpers C and C1 must be removed.)

Jumper	Definition
FD	Jumper inserted to enable Programmable Baud Rate.
M	Jumper inserted will assert the B BALC L on all received Framing Errors except when Maintenance Bit is set.
B, -B	B jumper inserted to assert B DCOK L on all received Framing Errors except when the Maintenance Bit is set. (-B jumper must be removed.)
1A,2A,3A	Jumpers inserted make the 20-A Current Loop receiver active. (Jumpers 1P and 2P must be removed.)
1P, 2P	Jumpers inserted make the 20mA Current Loop receiver passive. (Jumpers 1A, 2A and 3A must be removed.)
4A, 5A	Jumpers inserted make the 20mA Current Loop transmitter active. (Jumpers 3P and 4P must be removed.)
3P, 4P	Jumpers inserted make the 20mA Current Loop transmitter passive. (Jumpers 4A and 5A must be removed.)
-EF	Jumper removed enables the UART Error Flags to be read in the high byte of the Receiver Buffer.
MT	Jumper inserted to enable operation of the Maintenance Bit (TCSR bit 2).
M, M1	Manufacturing use only.

NOTE: Jumpers are labelled to indicate whether they are inserted or removed to enable their corresponding features.

(No additional marking) - Jumper inserted to enable feature.

("-" marking) - Jumper removed to enable feature.

TABLE 1

UART BAUD RATE SELECTIONS

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11 (See Note 1)
Program Control (TCSR)					
Receive Jumpers	R3	R2	R1	R0	
Transmit Jumpers	T3	T2	T1	T0	Baud Rate
	I	I	I	I	50
	I	I	I	R	75
	I	I	R	I	110
	I	I	R	R	134.5
	I	R	I	I	150
	I	R	I	R	300
	I	R	R	I	600
	I	R	R	R	1200
	R	I	I	I	1800
	R	I	I	R	2000
	R	I	R	I	2400
	R	I	R	R	3600
	R	R	I	I	4800
	R	R	I	R	7200
	R	R	R	I	9600
	R	R	R	R	19200 (See Note 2)

I = Jumper Inserted = Program Bit Cleared

R = Jumper Removed = Program Bit Set

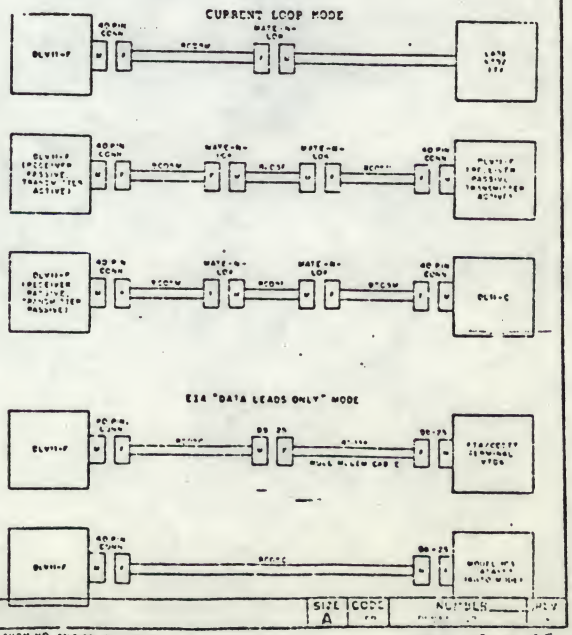
NOTE 1: Bit 11 of the TCSR (Write Only Bit) must also be set in order to select a new Baud Rate under program control. Also, jumper FD must be inserted to enable Baud Rate selection under program control.

NOTE 2: At 19.2K baud, actual clock frequency is 316.8 KHz (3.125% error).

6.2 Cable Configuration Example

FIGURE 1 illustrates the method of connecting cables between the DLV11A and associated external devices.

FIGURE 1



3.0 APPLICABLE DOCUMENTS

EIA Standard (RS-232-C)

D-CS-M8017

A-PS-1913040 (DC005)

A-PS-1912729 (DC004)

A-PS-1912730 (DC003)

A-PS-2112623 (5016)

DEC Std. 160 (LSI-11 Bus Specification)

DEC Std. 102 (Computer Environment Std.)

4.0 POWER REQUIREMENTS

	AMPS Typ	AMPS Max	WATTS Typ	WATTS Max
+5 Volt ± 5%	1.0 Amps	1.5 Amps	5W	7.5W
+12 Volt ± 3%	150mA	230mA	1.8W	2.8W

5.0 EXTERNAL CONNECTIONS

5.1 DLV11-F Edge Connector Pinning

+5	AA2	BIRQ L	AL2
	BA2		
+12	AD2		
BBSY L	AP2	BRPLY L	AF2
BDAL 0 L	AU2		
BDAL 1 L	AV2	BSYNC L	AJ2
BDAL 2 L	BE2		
BDAL 3 L	BF2	GND	AC2
BDAL 4 L	BH2	GND	AT1
BDAL 5 L	BJ2		
BDAL 6 L	BK2		
BDAL 7 L	BL2	GND	BC2
BDAL 8 L	BM2	BDCOK H	DA1
BDAL 9 L	BN2		
BDAL 10 L	BP2	GND	BT1
BDAL 11 L	BR2	MSPARE A -12V	AK1
BDAL 12 L	BS2	MSPARE A -12V	AL1
BDAL 13 L	BT2	MSPARE B	BK1
BDAL 14 L	BU2	MSPARE B (EXT B CLK)	BL1
BDAL 15 L	BV2		
BDIN L	AH2		
BDOUT L	AE2		
BHALT L	AP1		
BIAK 1 L*	AM2	SEPARI 3 (EXT T CLK)	BH1
BIAK 0 L*	AN2		
BINIT L	AT2		
BDMGIL*	AR2		
BDMGOL*	AS2		

* These signal pairs are not bussed bit pins through this module in order to propogate the daisy chain.

5.2 40-Pin Connector Pinning

Header Pin	M8028 Module	BC01V Moder Cable	BC05M 20mA Cable
A	Ground		
B	Ground		Ground
C	Force Busy(EIA)	Force Busy	
D			
E	Serial Input(TTL)	Interlock In <---	Interlock In
F	Serial Output(EIA)	Transmitted Data	
H	20mA Interlock		Interlock Out
J	Serial Input (EIA)	Received Data	
K	Serial Input+(20mA)		Received Data +
L		External Clock	
M	EIA Interlock	Interlock Out --->	
N		Serial Clock Xmit	
P			
R		Serial Clock Rcvr	
S	Serial Input-(20mA)		Received Data -
T		Clear to Send	
U			
V	Request to Send (EIA)	Request to Send	
W			
X		Ring	
Y			
Z		Data Set Ready	
AA	Serial Output+(20mA)		Transmitted Data+
BB		Carrier	
CC	Clock Input (TTL)		
DD	Data Terminal Rdy (EIA)	Data Terminal Rdy	
EE	Reader Run-(20mA)		Reader Run -
FF		202 Sec Xmit	
HH	Serg Clock Enb		
JJ		202 Sec Rcvr	
KK	Serial Output-(20mA)		Transmitted Data-
LL			
MM			
NN			
PP	Reader Run+(20mA)		Reader Run +
RR			
SS	Serial Output(TTL)		
TT	+5V		
UU	Ground		Ground
VV	Ground	Ground	Ground

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION — DATE 6 MARCH 79

TITLE DLV11-F ENGINEERING SPECIFICATION

REVISIONS

REV	DESCRIPTION	ECO NO	ORIG	DATE	APPD BY	DATE

ENGR [illegible] APPD [illegible] | SIZE A | CODE [illegible] | NUMBER DLV11-F | REV

SHEET 1 OF 25

TABLE OF CONTENTS

1.0 SCOPE

The scope of this document is to present the description and specification for the DLV11-F (M8028 Asynchronous Line Interface. It describes the DLV11-F both physically and functionally.

2.0 GENERAL DESCRIPTION

The DLV11-F is an interface between an asynchronous serial line and the LSI-11 Bus. The LSI-11 Bus circuitry is designed in accordance with DEC Std 160, "LSI-11 Bus Specification". All circuitry is housed on one dual extended height module (M8028) and mounts in any standard LSI-11 backplane. The DLV11-F supports the following two modes of operation:

1. Current Loop Mode

   20mA current loop circuits are supplied to the external device via a female MATE-N-LOCK connector when used with the BC05M-XX cable.

2. EIA "Data Leads Only" Mode

   EIA drivers and receivers are supplied to the external device via a male DB25 connector used with the BC01V-XX cable.

Kanalunabhängige Brücken

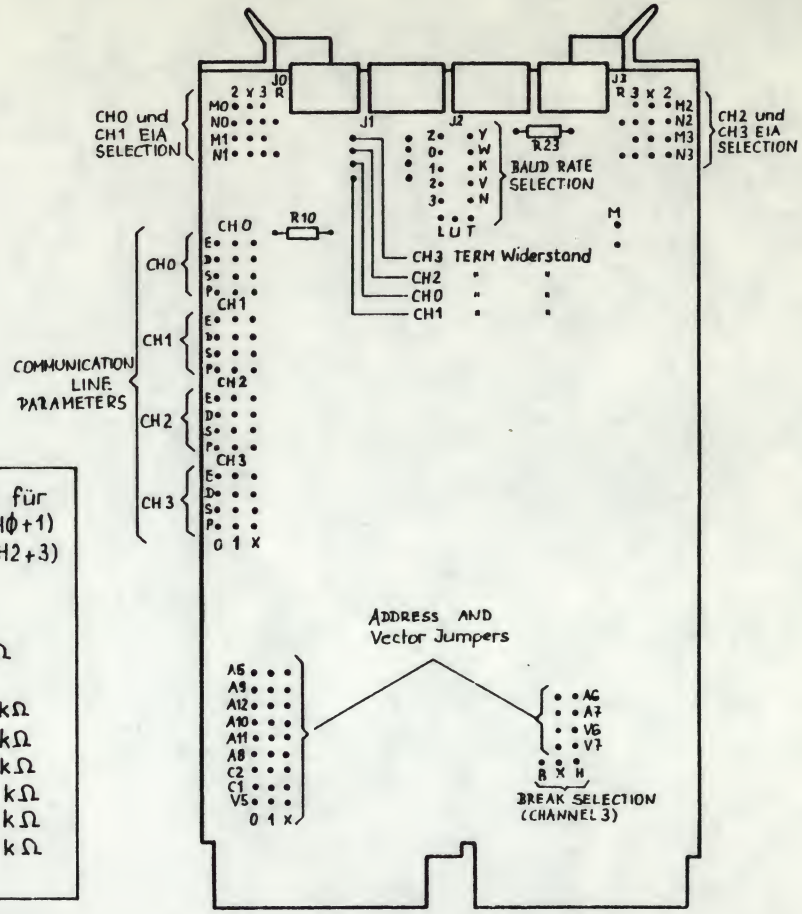
Brücke	Bed	Stellung	Std	Anw	Brücke	Bed.	Stellung	Std.	Anw	Brücke	Bed	Stellung	Std.	Anw
A12	Basis-Adresse	X-0 X-1	X		A6	Adr.	R J	X		C1	Konsole auf	X-0 X-1	X	
A11		X-0 X-1	X		A5		X-0 X-1	X		C2	CH3	X-0 X-1	X	
A10		X-0 X-1	X		V7	Basis-Vec	R J	X		Break Reakt. CH3	Inh. Halt Boot	R X-H X-B	X	
A9		X-0 X-1	X		V6		R J	X						
A8		X-0 X-1	X		V5		X-0 X-1			R10	Impulsformung bei V24 je nach Baud-Rate (Tabelle)		120k	
A7		R J	X		M	Konsole	R J	X		R23			120k	

Std.-Adr. 177500 | Anw.-Adr.: | Std.-Vec: 300 | Anw.-Vec:

Einstellung je Kanal		Ø			1			2			3		
Brücke	Bedeutung	Stellung	Std	Anw	Stellung	Std	Anw	Stellung	Std	Anw	Stellung	Std.	Anw
Baud-rate	150 bd	0-U			1-U			2-U			3-U		
	300 bd	0-T			1-T			2-T			3-T		
	600 bd	0-V			1-V			2-V			3-V		
	1,2 kbd	0-W			1-W			2-W			3-W		
	2,4 kbd	0-Y			1-Y			2-Y			3-Y		
	4,8 kbd	0-L			1-L			2-L			3-L		
	9,6 kbd	0-N	x		1-N	x		2-N	x		3-N	x	
	19,2 kbd	0-K			1-K			2-K			3-K		
	38,4 kbd	0-Z			1-Z			2-Z			3-Z		
D	7 Datenbits	X-0			X-0			X-0			X-0		
	8 Datenbits	X-1	X		X-1	X		X-1	X		X-1	X	
S	1 Stop Bit	X-0			X-0			X-0			X-0		
	2 Stop Bits	X-1	X		X-1	X		X-1	X		X-1	X	
P	Parity enable	X-0			X-0			X-0			X-0		
	Parity inhibit	X-1	X		X-1	X		X-1	X		X-1	X	
E	Odd Parity	X-0			X-0			X-0			X-0		
	Even Parity	X-1	X		X-1	X		X-1	X		X-1	X	
M+N TERM	Ü-Norm EIA RS 422	X-2 100Ω			X-2 100Ω			X-2 100Ω			X-2 100Ω		
M+N	Ü-Norm V24	X-3			X-3			X-3			X-3		
M	Ü-Norm 20mA mit 900.611	X-3	X		X-3	X		X-3	X		X-3	X	
N	Ü-Norm 20mA mit 900.611	X-R	X		X-R	X		X-R	X		X-R	X	

Tabelle für R10 (CHØ+1) R23 (CH2+3)

1MΩ	
820 kΩ	
430 kΩ	
200 kΩ	
120 kΩ	
51 kΩ	
22 kΩ	



R = entfernt

J = eingesetzt

					Freimaßtoleranzen		
					78	Tag	Name
					Bearb.	27.11.	Mü/Ber
					Gepr.	28.11.	Nk
					Norm		
a	369	6.12.78	Mü				
Änd.	Änderung	Tag	Name		PERIPHERE COMPUTER SYSTEME		

Standard: Bildschirm-Terminals (3=Konsole)
Anwendung:

Einstell - Tabelle für DLV 11 - J (M8043)

Maßstab

B 900.610.3